Delson
Technology Co, Ltd.

# D73CAG02168CG
# HIGH PERFORMANCE 1Gbit DDR3 SDRAM
# 8 BANKS X 16Mbit X 16

## Feature

- 1.5V ± 0.075V / 1.35V -0.0675V/+0.1V (JEDEC Standard Power Supply)
- 8 Internal memory banks (BA0- BA2)
- Differential clock input (CK, $\overline{CK}$)
- Programmable $\overline{CAS}$ Latency: 6, 7, 8, 9, 10, 11
- Programmable Additive Latency: 0, CL-1, CL-2
- Programmable Sequential / Interleave Burst Type
- Programmable Burst Length: 4, 8
- 8 bit prefetch architecture
- Output Driver Impedance Control
- Write Leveling
- OCD Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- Auto Self-Refresh
- Self-Refresh Temperature
- RoHS compliance and Halogen free
- Packages:

78-Ball BGA for x4 & x8 components

96-Ball BGA for x16 components

## Description

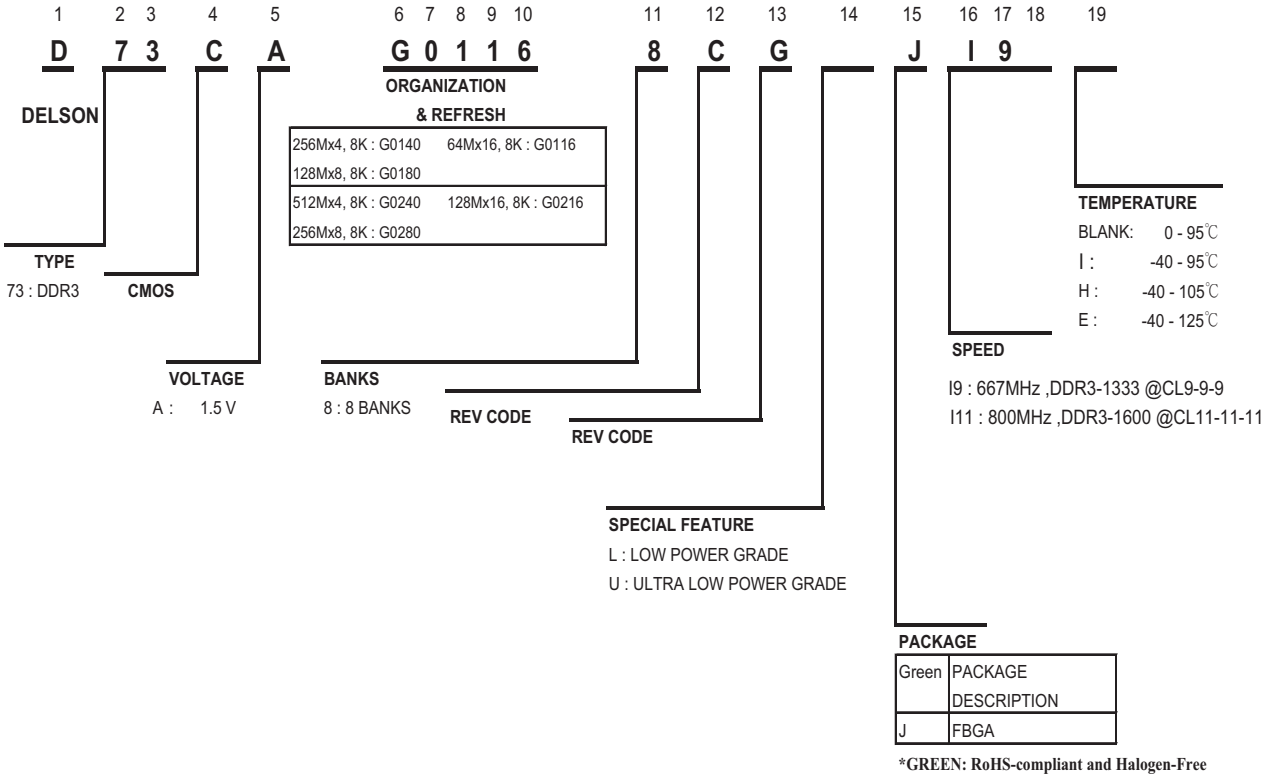
The 2Gb Double-Data-Rate-3 (DDR3) DRAMs is a high-speed CMOS Double Data Rate32 SDRAM containing 2,147,483,648 bits. It is internally configured as an octal-bank DRAM.

The 2Gb chip is organized as 64Mbit x 4 I/O x 8 bank, 32Mbit x 8 I/O x 8 bank or 16Mbit x 16 I/O x 8 bank device. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1600 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3 DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.5V ± 0.075V and 1.35V -0.0675V/+0.1V power supply and are available in BGA packages.

### *Part Number Information*




***GREEN: RoHS-compliant and Halogen-Free**

## Pin Configuration – 78 balls BGA Package (x8)

< TOP View>

See the balls through the package

x 8

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VSS | VDD | NC | A | NU/$\overline{\text{TDQS}}$ | VSS | VDD |
| VSS | VSSQ | DQ0 | B | DM/TDQS | VSSQ | VDDQ |
| VDDQ | DQ2 | DQS | C | DQ1 | DQ3 | VSSQ |
| VSSQ | DQ6 | $\overline{\text{DQS}}$ | D | VDD | VSS | VSSQ |
| VREFDQ | VDDQ | DQ4 | E | DQ7 | DQ5 | VDDQ |
| NC | VSS | $\overline{\text{RAS}}$ | F | CK | VSS | NC |
| ODT | VDD | $\overline{\text{CAS}}$ | G | $\overline{\text{CK}}$ | VDD | CKE |
| NC | $\overline{\text{CS}}$ | $\overline{\text{WE}}$ | H | A10/AP | ZQ | NC |
| VSS | BA0 | BA2 | J | NC | VERFCA | VSS |
| VDD | A 3 | A 0 | K | A12/ $\overline{\text{BC}}$ | BA1 | VDD |
| VSS | A 5 | A2 | L | A1 | A4 | VSS |
| VDD | A7 | A9 | M | A11 | A6 | VDD |
| VSS | $\overline{\text{RESET}}$ | A13 | N | A14 | A8 | VSS |

## Pin Configuration – 96 balls BGA Package (x16)

< TOP View>

See the balls through the package

x 16

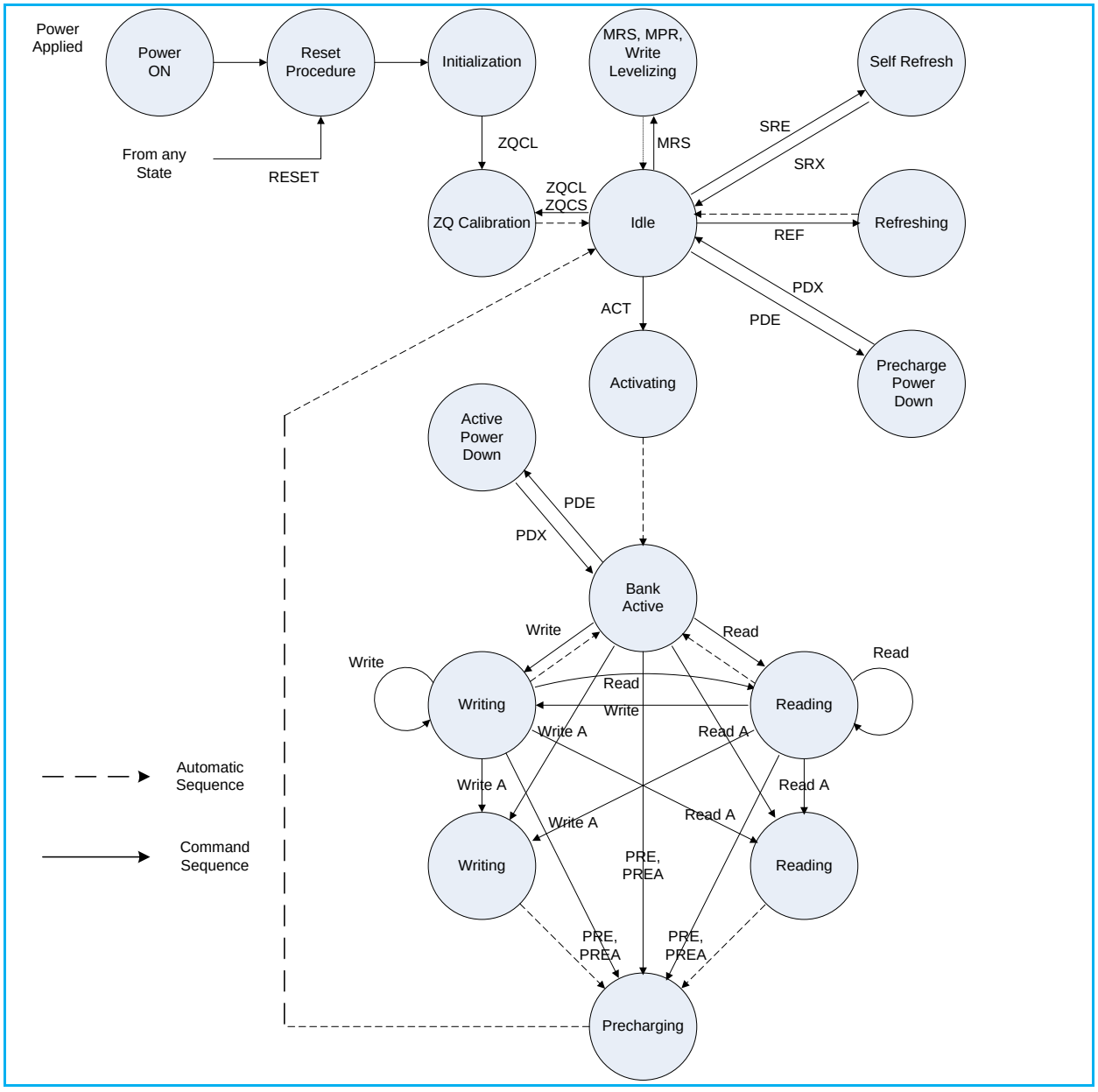
| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VDDQ | DQU5 | DQU7 | A | DQU4 | VDDQ | VSS |
| VSSQ | VDD | VSS | B | $\overline{\text{DQSU}}$ | DQU6 | VSSQ |
| VDDQ | DQU3 | DQU1 | C | DQSU | DQU2 | VDDQ |
| VSSQ | VDDQ | UDM | D | DQU0 | VSSQ | VDD |
| VSS | VSSQ | DQL0 | E | DML | VSSQ | VDDQ |
| VDDQ | DQL2 | DQSL | F | DQL1 | DQL3 | VSSQ |
| VSSQ | DQL6 | $\overline{\text{DQSL}}$ | G | VDD | VSS | VSSQ |
| VREFDQ | VDDQ | DQL4 | H | DQL7 | DQL5 | VDDQ |
| NC | VSS | $\overline{\text{RAS}}$ | J | CK | VSS | NC |
| ODT | VDD | $\overline{\text{CAS}}$ | K | $\overline{\text{CK}}$ | VDD | CKE |
| NC | $\overline{\text{CS}}$ | $\overline{\text{WE}}$ | L | A10/AP | ZQ | NC |
| VSS | BA0 | BA2 | M | A15 | VREFCA | VSS |
| VDD | A3 | A0 | N | A12/BC# | BA1 | VDD |
| VSS | A5 | A2 | P | A1 | A4 | VSS |
| VDD | A7 | A9 | R | A11 | A6 | VDD |
| VSS | $\overline{\text{RESET}}$ | A13 | T | A14 | A8 | VSS |

## Input / Output Functional Description

| Symbol | Type | Function |
|---|---|---|
| CK, $\overline{CK}$ | Input | **Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. |
| CKE | Input | **Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After $V_{REF}$ has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, $V_{REF}$ must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh. |
| $\overline{CS}$ | Input | **Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | **Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered. |
| DM, (DMU, DML) | Input | **Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS / $\overline{TQDS}$ is enabled by Mode Register A11 setting in MR1 |
| BA0 - BA2 | Input | **Bank Address Inputs:** BA0, BA1, and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle. |
| A0 – A14 | Input | **Address Inputs:** Provide the row address for Activate commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional function as below. The address inputs also provide the op-code during Mode Register Set commands. |
| A12 / $\overline{BC}$ | Input | **Burst Chop:** A12/$\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on the fly) will be performed. (HIGH - no burst chop; LOW - burst chopped). |
| DQ | Input/output | **Data Inputs/Output:** Bi-directional data bus. |
| DQL,<br>DQU,<br>DQS,($\overline{DQS}$),<br>DQSL,($\overline{DQSL}$),<br>DQSU,($\overline{DQSU}$), | Input/output | **Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. The data strobes DQS, DQSL, DQSU are paired with differential signals $\overline{DQS}$, $\overline{DQSL}$, $\overline{DQSU}$, respectively, to provide differential pair signaling to the system during both reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended. |

| Symbol | Type | Function |
|---|---|---|
| ODT | Input | **On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (when TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if Mode-registers, MR1and MR2, are programmed to disable RTT. |
| $\overline{RESET}$ | Input | **Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V |
| NC | | **No Connect:** No internal electrical connection is present. |
| $V_{DDQ}$ | Supply | **DQ Power Supply:** 1.5V ± 0.075V , 1.35V -0.0675V/+0.1V |
| $V_{DD}$ | Supply | **Power Supply:** 1.5V ± 0.075V, 1.35V -0.0675V/+0.1V |
| $V_{SSQ}$ | Supply | **DQ Ground** |
| $V_{SS}$ | Supply | **Ground** |
| $V_{REFCA}$ | Supply | **Reference voltage for CA** |
| $V_{REFDQ}$ | Supply | **Reference voltage for DQ** |
| ZQ | Supply | **Reference pin for ZQ calibration.** |
| Note: Input only pins (BA0-BA2, A0-A13, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, and $\overline{RESET}$) do not supply termination. | | |

## Simplified State Diagram




| Abbreviation | Function | Abbreviation | Function | Abbreviation | Function |
|---|---|---|---|---|---|
| ACT | Active | Read | RD, RDS4, RDS8 | PED | Enter Power-down |
| PRE | Precharge | Read A | RDA, RDAS4, RDAS8 | PDX | Exit Power-down |
| PREA | Precharge All | Write | WR, WRS4, WRS8 | SRE | Self-Refresh entry |
| MRS | Mode Register Set | Write A | WRA, WRAS4, WRAS8 | SRX | Self-Refresh exit |
| REF | Refresh | $\overline{\text{RESET}}$ | Start RESET Procedure | MPR | Multi-Purpose Register |
| ZQCL | ZQ Calibration Long | ZQCS | ZQ Calibration Short | - | - |

# Basic Functionality

The DDR3 SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A13 select the row). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BC8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

## DRAM Initialization and RESET

Power-up Initialization sequence

The Following sequence is required for POWER UP and Initialization

1. Apply power ($\overline{\text{RESET}}$ is recommended to be maintained below 0.2 x VDD, all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200μs with stable power. CKE is pulled "Low" anytime before $\overline{\text{RESET}}$ being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to $VDD_{min}$ must be no greater than 200ms; and during the ramp, VDD>VDDQ and (VDD-VDDQ) <0.3 Volts.
- VDD and VDDQ are driven from a single power converter output, AND
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished, AND
- $V_{ref}$ tracks VDDQ/2.

OR
- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & $V_{ref}$.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

3. Clock (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock ($t_{IS}$) must be meeting. Also a NOP or Deselect command must be registered (with $t_{IS}$ set up time to clock) before CKE goes active. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of $t_{DLLK}$ and $t_{ZQinit}$.

4. The DDR3 DRAM will keep its on-die termination in high impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the DRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ de-assertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. [tXPR=max(tXS, 5tCK)]

6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1)

7. Issue MRS command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1)

8. Issue MRS command to load MR1 with all application settings and DLL enabled. (To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to BA1 and BA2)

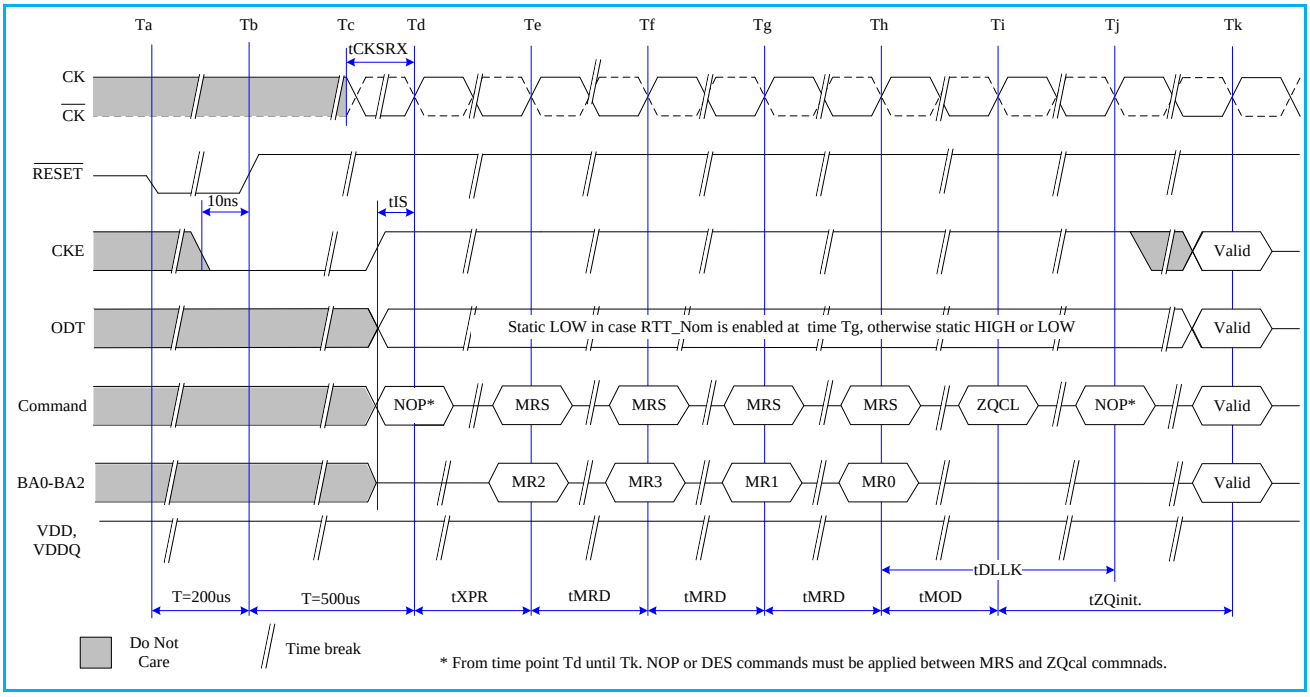
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0-BA2)

10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both $t_{DLLK}$ and $t_{ZQinit}$ completed.

12. The DDR3 SDRAM is now ready for normal operation.

### DDR3 Reset and Initialization Sequence at Power-on Ramping



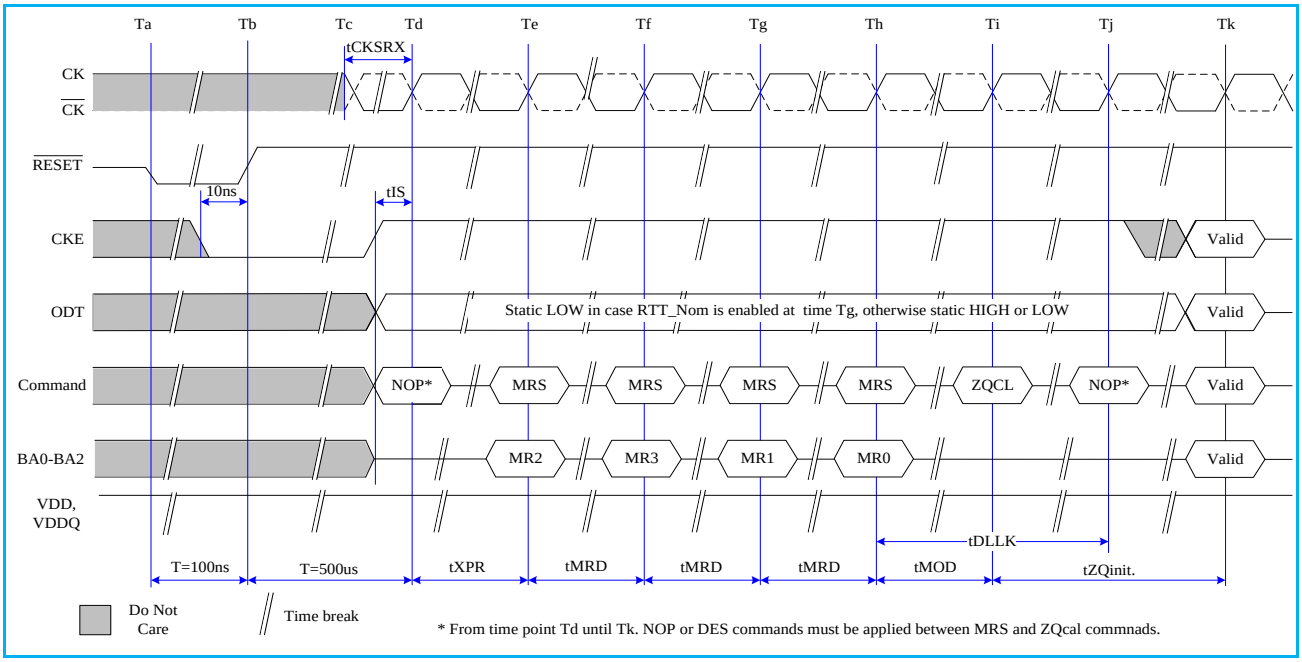

## DDR3 Reset Procedure at Power Stable Condition

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2*VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100ns. CKE is pulled “Low” before RESET being de-asserted (min. time 10ns).

2. Follow Power-up Initialization Sequence step 2 to 11.

3. The Reset sequence is now completed. DDR3 SDRAM is ready for normal operation.

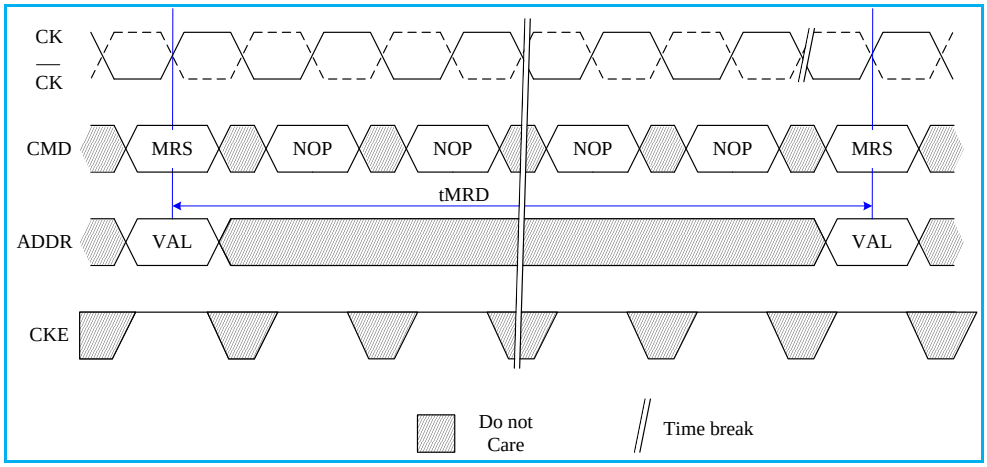


## Register Definition

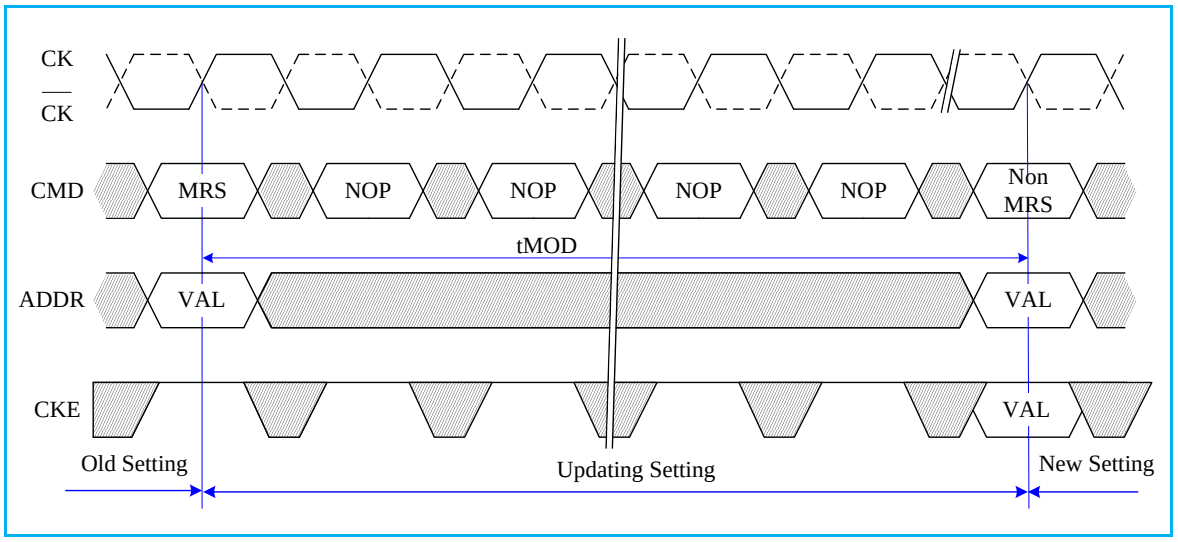
## Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents

The mode register set command cycle time, $t_{MRD}$ is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown as below.




The MRS command to Non-MRS command delay, tMOD, is require for the DRAM to update the features except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown as the following figure.



The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

The mode-register MR0 stores data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR, and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

## MR0 Definition

Address Filed

| BA2* | BA1 | BA0 | A13* | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**MRS mode**

| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | **MR0** |
| 0 | 1 | **MR1** |
| 1 | 0 | **MR2** |
| 1 | 1 | **MR3** |

**Burst Length**

| A1 | A0 | BL |
|---|---|---|
| 0 | 0 | 8 (Fixed) |
| 0 | 1 | BC4 or 8 (on the fly) |
| 1 | 0 | BC4 (Fixed) |
| 1 | 1 | Reserved |

**Precharge Power Down**

| A12 | DLL Control for Precharge PD |
|---|---|
| 0 | Slow Exit (Low Power) |
| 1 | Fast Exit (Normal) |

**Burst Type**

| A3 | Burst Type |
|---|---|
| 0 | Nibble Sequential |
| 1 | Interleave |

**Write recovery for autoprecharge****

| A11 | A10 | A9 | WR(cycles) |
|---|---|---|---|
| 0 | 0 | 0 | 16 |
| 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 6 |
| 0 | 1 | 1 | 7 |
| 1 | 0 | 0 | 8 |
| 1 | 0 | 1 | 10 |
| 1 | 1 | 0 | 12 |
| 1 | 1 | 1 | 14 |

**CAS Latency**

| A6 | A5 | A4 | A2 | CAS Latency |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 0 | 5 |
| 0 | 1 | 0 | 0 | 6 |
| 0 | 1 | 1 | 0 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 1 | 0 | 9 |
| 1 | 1 | 0 | 0 | 10 |
| 1 | 1 | 1 | 0 | 11 |

**DLL Reset**

| A8 | DLL Reset |
|---|---|
| 0 | NO |
| 1 | YES |

**Mode**

| A7 | Mode |
|---|---|
| 0 | Normal |
| 1 | TEST |

* BA2 and A13 are reserved for future use and must be set to 0 when programming the MR.
**WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR (ns) by tCK (ns) and rounding up to the next integer: Wrmin[cycles] = Roundup(tWR/tCK). The value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

## Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in the MR0 Definition as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length is defined by bits A0-A1. Burst lengths options include fix BC4, fixed BL8, and on the fly which allow BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/$\overline{BC}$.

## Burst Type and Burst Order

| Burst Length | Read Write | Starting Column Address (A2,A1,A0) | Burst type: Sequential (decimal) A3 = 0 | Burst type: Interleaved (decimal) A3 = 1 | Note |
|---|---|---|---|---|---|
| 4 Chop | Read | 0 , 0 , 0 | 0,1,2,3,T,T,T,T | 0,1,2,3,T,T,T,T | 1,2,3 |
| | | 0 , 0 , 1 | 1,2,3,0,T,T,T,T | 1,0,3,2,T,T,T,T | |
| | | 0 , 1 , 0 | 2,3,0,1,T,T,T,T | 2,3,0,1,T,T,T,T | |
| | | 0 , 1 , 1 | 3,0,1,2,T,T,T,T | 3,2,1,0,T,T,T,T | |
| | | 1 , 0 , 0 | 4,5,6,7,T,T,T,T | 4,5,6,7,T,T,T,T | |
| | | 1 , 0 , 1 | 5,6,7,4,T,T,T,T | 5,4,7,6,T,T,T,T | |
| | | 1 , 1 , 0 | 6,7,4,5,T,T,T,T | 6,7,4,5,T,T,T,T | |
| | | 1 , 1 , 1 | 7,4,5,6,T,T,T,T | 7,6,5,4,T,T,T,T | |
| | Write | 0 , V , V | 0,1,2,3,X,X,X,X | 0,1,2,3,X,X,X,X | 1,2,4,5 |
| | | 1 , V , V | 4,5,6,7,X,X,X,X | 4,5,6,7,X,X,X,X | |
| 8 | Read | 0 , 0 , 0 | 0,1,2,3,4,5,6,7 | 0,1,2,3,4,5,6,7 | 2 |
| | | 0 , 0 , 1 | 1,2,3,0,5,6,7,4 | 1,0,3,2,5,4,7,6 | |
| | | 0 , 1 , 0 | 2,3,0,1,6,7,4,5 | 2,3,0,1,6,7,4,5 | |
| | | 0 , 1 , 1 | 3,0,1,2,7,4,5,6 | 3,2,1,0,7,6,5,4 | |
| | | 1 , 0 , 0 | 4,5,6,7,0,1,2,3 | 4,5,6,7,0,1,2,3 | |
| | | 1 , 0 , 1 | 5,6,7,4,1,2,3,0 | 5,4,7,6,1,0,3,2 | |
| | | 1 , 1 , 0 | 6,7,4,5,2,3,0,1 | 6,7,4,5,2,3,0,1 | |
| | | 1 , 1 , 1 | 7,4,5,6,3,0,1,2 | 7,6,5,4,3,2,1,0 | |
| | Write | V , V , V | 0,1,2,3,4,5,6,7 | 0,1,2,3,4,5,6,7 | 2,4 |

Note:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/$\overline{BC}$, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0~7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Do not Care.

## CAS Latency

The CAS Latency is defined by MR0 (bit A9~A11) as shown in the MR0 Definition figure. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

## Test Mode

The normal operating mode is selected by MR0 (bit7=0) and all other bits set to the desired values shown in the MR0 definition figure. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM manufacturer and should not be used. No operations or functionality is guaranteed if A7=1.

## DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Anytime the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.)

## Write Recovery

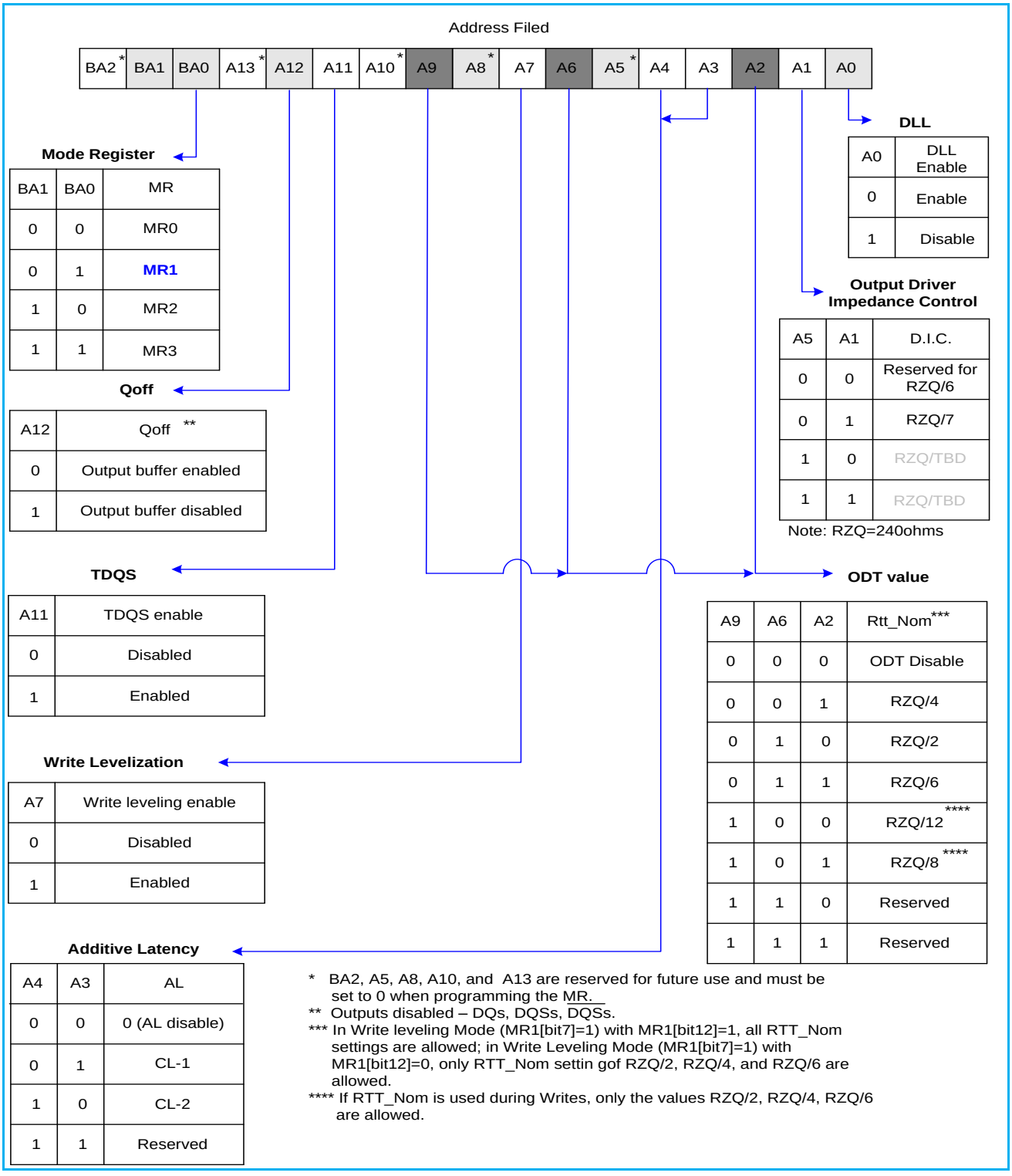
The programmed WR value MR0(bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR (write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(ns) by tCK(ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal or larger than tWR(min).

## Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12=0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12=1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

## Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output strength, Rtt_Nom impedance, additive latency, WRITE leveling enable and Qoff. The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the following figure.



## DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0=0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enable upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, expect when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation in DLL-off Mode.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10,A9}={0,0}, to disable Dynamic ODT externally.

## Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1(bit A1 and A5) as shown in MR1 definition figure.

## ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmable in MR1. A separate value (Rtt_WR) may be programmable in MR2 to enable a unique Rtt value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

## Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidth in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown as the following table.

## Additive Latency (AL) Settings

| A4 | A3 | AL |
|---|---|---|
| 0 | 0 | 0, (AL Disable) |
| 0 | 1 | CL-1 |
| 1 | 0 | CL-2 |
| 1 | 1 | Reserved |

## Write leveling

For better signal integrity, DDR3 memory module adopted fly by topology for the commands, addresses, control signals, and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the controller should support 'write leveling' in DDR3 SDRAM to compensate for skew.

## Output Disable

The DDR3 SDRAM outputs maybe enable/disabled by MR1 (bit12) as shown in MR1 definition. When this feature is enabled (A12=1) all output pins (DQs, DQS, $\overline{DQS}$, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring modules power for example. For normal operation A12 should be set to '0'.

## TDQS, $\overline{TDQS}$

TDQS (Termination Data Strobe) is a feature of x8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in x4 configurations. When enabled via the mode register, the same termination resistance function is applied to be TDQS/$\overline{TDQS}$ pins that are applied to the DQS/$\overline{DQS}$ pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the $\overline{TDQS}$ pin is not used.

The TDQS function is available in x8 DDR3 SDRAM only and must be disabled via the mode register A11=0 in MR1 for x4 configurations.

## TDQS, $\overline{TDQS}$ Function Matrix

| MR1 (A11) | DM / TDQS | NU / TDQS |
|---|---|---|
| 0 (TDQS Disabled) | DM | Hi-Z |
| 1 (TDQS Enabled) | TDQS | TDQS |
| Note: | | |
| 1. If TDQS is enabled, the DM function is disabled. | | |
| 2. When not used, TDQS function can be disabled to save termination power. | | |
| 3. TDQS function is only available for x8 DRAM and must be disabled for x4 | | |

# Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

Address Filed

| BA2 * | BA1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**MRS mode**

| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | **MR0** |
| 0 | 1 | **MR1** |
| 1 | 0 | **MR2** |
| 1 | 1 | **MR3** |

**Rtt_WR****

| A10 | A9 | **Rtt_WR** |
|---|---|---|
| 0 | 0 | **Dynamic ODT off (Write does not affect RTT value )** |
| 0 | 1 | **RZQ/4** |
| 1 | 0 | **RZQ/2** |
| 1 | 1 | **Reserved** |

**Self-Refresh Temperature Range**

| A7 | SRT |
|---|---|
| 0 | Normal Operating temperature range |
| 1 | Extended operating temperature range |

**Auto Self Refresh**

| A6 | ASR |
|---|---|
| 0 | Manual Self Refresh Reference |
| 1 | ASR Enable |

**PASR**

| A2 | A1 | A0 | PASR |
|---|---|---|---|
| 0 | 0 | 0 | Full Array |
| 0 | 0 | 1 | Half Array (000,001,010,011 ) |
| 0 | 1 | 0 | Quarter Array (000,001) |
| 0 | 1 | 1 | 1/8th Array (000) |
| 1 | 0 | 0 | 3/4 array (010, 011, 100, 101, 110 , 111) |
| 1 | 0 | 1 | Half array (100, 101, 110, 111) |
| 1 | 1 | 0 | Quarter array (110, 111) |
| 1 | 1 | 1 | 1/8th array (111) |

**CAS Write Latency**

| A5 | A4 | A3 | CAS Write Latency |
|---|---|---|---|
| 0 | 0 | 0 | 5 (tCK(avg)>=2.5ns) |
| 0 | 0 | 1 | 6 (2.5ns>tCK(avg)>=1.875ns) |
| 0 | 1 | 0 | 7 (1.875ns>tCK(avg)>=1.5ns) |
| 0 | 1 | 1 | 8 (1.5ns>tCK(avg)>=1.25ns) |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

* BA2, A5, A8, A13 are reserved for future use and must be set to 0 when programming the MR .
** The Rtt _WR value can be applied during writes even when Rtt _Nom is disabled . During write leveling , Dynamic ODT is not available .

## CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5) shown in MR2. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 DRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL=AL+CWL.

## Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

DDR3 SDRAM must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.

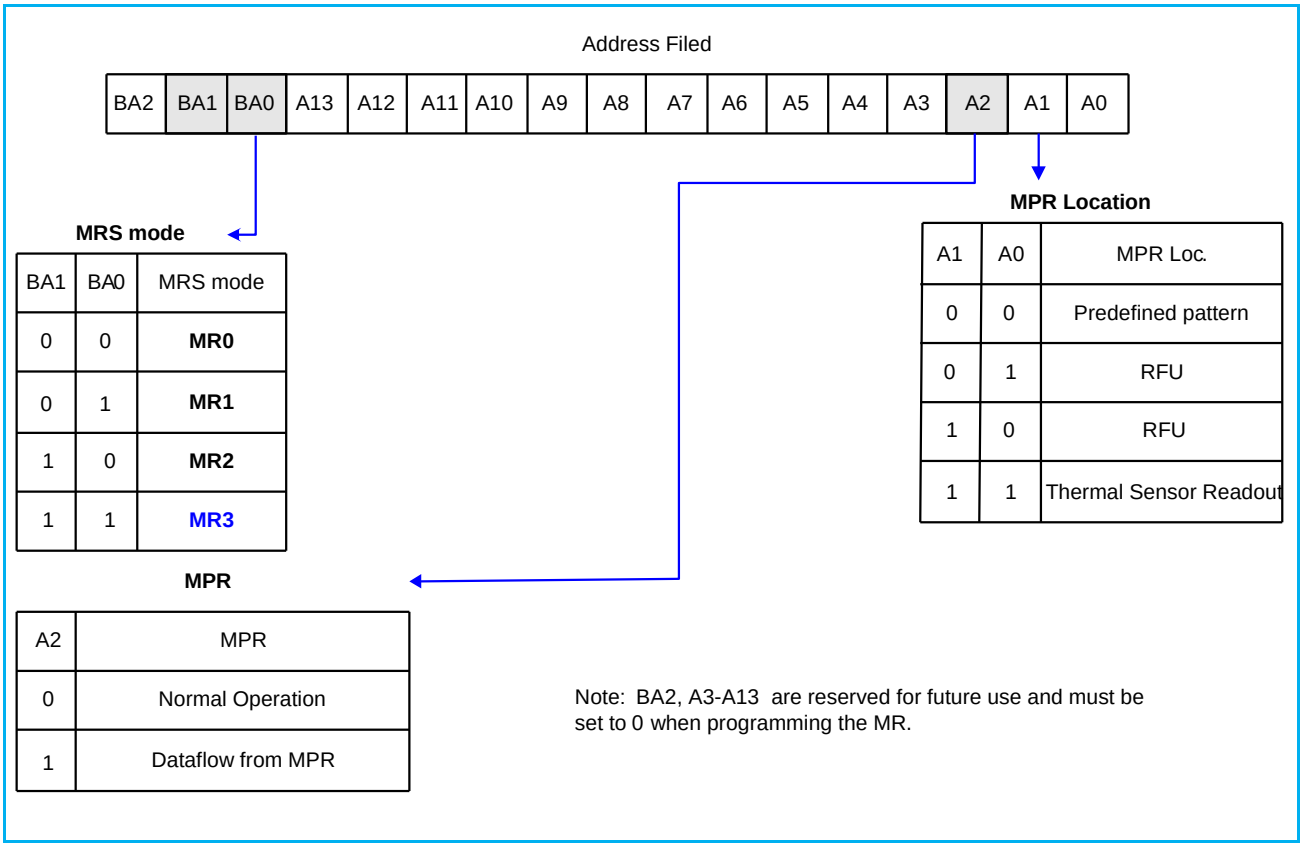
Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to “Extended Temperature Usage” on page48. DDR3 SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

## Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings

## Mode Register MR3

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.




| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | **MR0** |
| 0 | 1 | **MR1** |
| 1 | 0 | **MR2** |
| 1 | 1 | **MR3** |

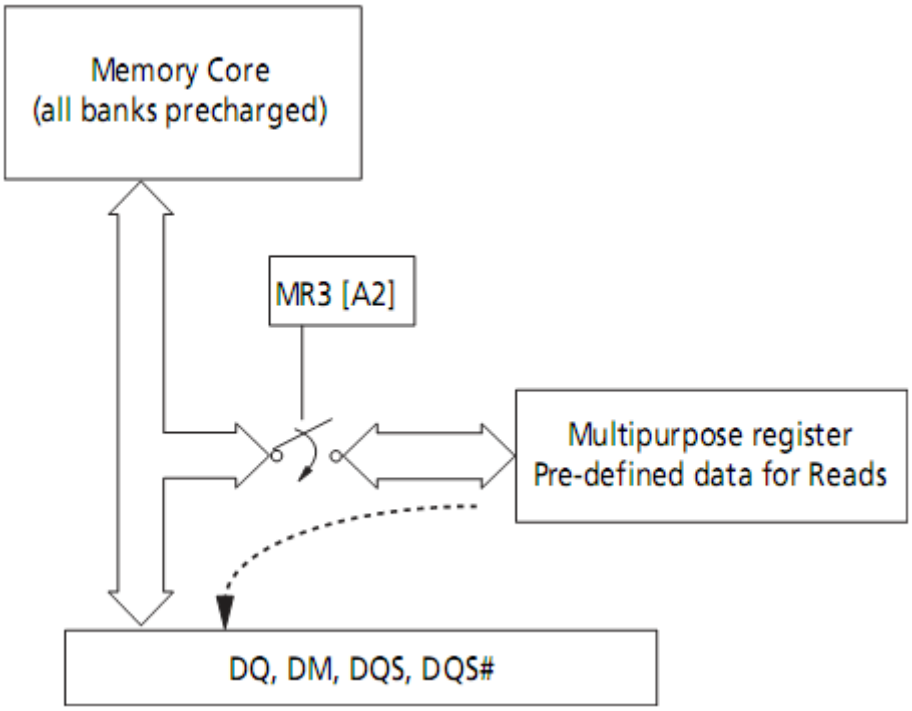
| A1 | A0 | MPR Loc. |
|---|---|---|
| 0 | 0 | Predefined pattern |
| 0 | 1 | RFU |
| 1 | 0 | RFU |
| 1 | 1 | Thermal Sensor Readout |

| A2 | MPR |
|---|---|
| 0 | Normal Operation |
| 1 | Dataflow from MPR |

Note: BA2, A3-A13 are reserved for future use and must be set to 0 when programming the MR.

## Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a Mode Register Set (MRS) command must be issued to MR3 register with bit A2=1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2=0). Power down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.




To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as shown in Table12. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table13. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

## DDR3 SDRAM Command Description and Operation

## Command Truth Table (Conti.)

NOTE1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.

NOTE2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.

NOTE5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE6. The Power-Down Mode does not perform any refresh operation.

NOTE7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE8. Self Refresh Exit is asynchronous.

NOTE9. VREF(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.

NOTE10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.

NOTE11. The Deselect command performs the same function as No Operation command.

NOTE12. Refer to the CKE Truth Table for more detail with CKE transition.

## CKE Truth Table

| Current State | CKE | | Command (N) | Action (N) | Notes |
|---|---|---|---|---|---|
| | Previous Cycle (N-1) | Current Cycle (N) | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$ | | |
| Power-Down | L | L | X | Maintain Power-Down | |
| | L | H | DESELECT or NOP | Power-Down Exit | |
| Self-Refresh | L | L | X | Maintain Self-Refresh | |
| | L | H | DESELECT or NOP | Self-Refresh Exit | |
| Bank(s) Active | H | L | DESELECT or NOP | Active Power-Down Entry | |
| Reading | H | L | DESELECT or NOP | Power-Down Entry | |
| Writing | H | L | DESELECT or NOP | Power-Down Entry | |
| Precharging | H | L | DESELECT or NOP | Power-Down Entry | |
| Refreshing | H | L | DESELECT or NOP | Precharge Power-Down Entry | |
| All Banks Idle | H | L | DESELECT or NOP | Precharge Power-Down Entry | |
| | H | L | REFRESH | Self-Refresh | |

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registrations. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh modes can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are NOP and DESELECT only.

NOTE 13 Self-Refresh cannot be entered during Read or Write operations.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15“X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

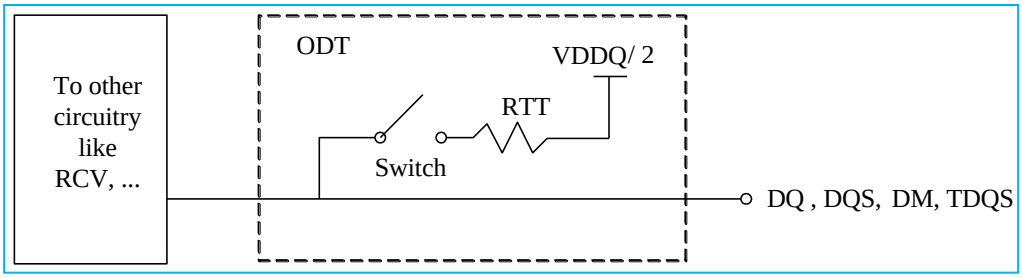
NOTE 18‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.)

## On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{\text{DQS}}$, and DM for x4 and x8 configuration and TDQS, $\overline{\text{TDQS}}$ for x8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown as below.




The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of RTT is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Register MR1 and MR2 are programmed to disable ODT and in self-refresh mode.

## ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 {A2, A6, A9} or MR2 {A9, A10} are non-zero. In this case, the value of RTT is determined by the settings of those bits.

Application: Controller sends WR command together with ODT asserted.

One possible application: The rank that is being written to provides termination.

DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR)

DRAM does not use any write or read command decode information.

## Termination Truth Table

| ODT pin | DRAM Termination State |
|---|---|
| 0 | OFF |
| 1 | ON, (OFF, if disabled by MR1 {A2, A6, A9} and MR2{A9, A10} in general) |

## Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

Any bank active with CKE high

Refresh with CKE high

Idle mode with CKE high

Active power down mode (regardless of MR0 bit A12)

Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLonn = WL - 2; ODTLoff = WL-2.

## ODT Latency and Posted ODT

In synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2; ODTLoff = CWL + AL - 2. For details, refer to DDR3 SDRAM latency definitions.

## ODT Latency

| Symbol | Parameter | DDR3 SDRAM | Unit |
|---|---|---|---|
| ODTLon | ODT turn on Latency | WL - 2 = CWL + AL - 2 | tCK |
| ODTLoff | ODT turn off Latency | WL - 2 = CWL + AL - 2 | tCK |

## Timing Parameters

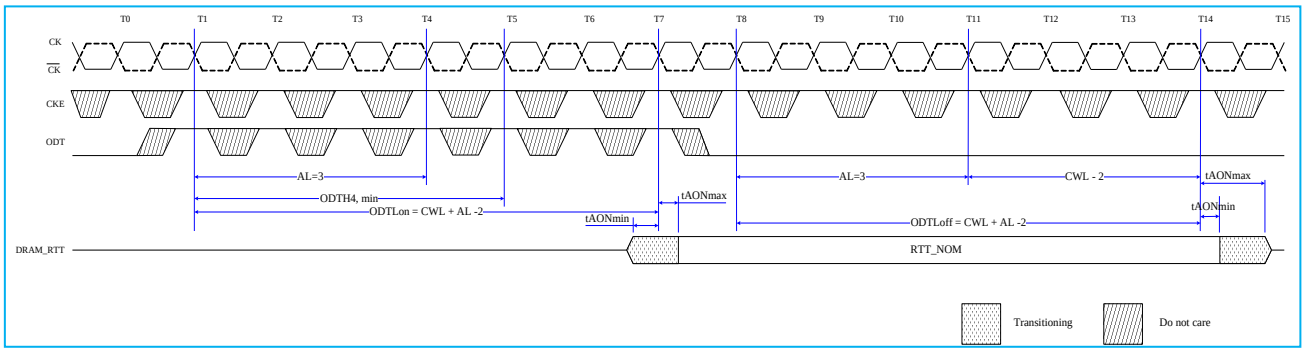
In synchronous ODT mode, the following timing parameters apply: ODTLon, ODTLoff, tAON min/max, AOF min/max.

Minimum RTT turn-on time (tAON min) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn-on time (tAON max) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

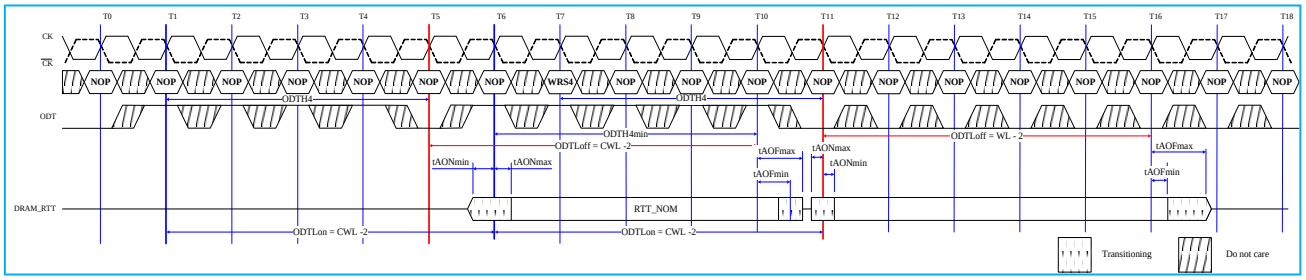
Minimum RTT turn-off time (tAOF min) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (tAOF max) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL=4) or ODTH8 (BL=8) after the write command. ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a write command until ODT is registered low.

## Synchronous ODT Timing Example for AL=3; CWL=5; ODTLon=AL+CWL-2=6; ODTLoff=AL+CWL-2=6




## Synchronous ODT example with BL=4, WL=7

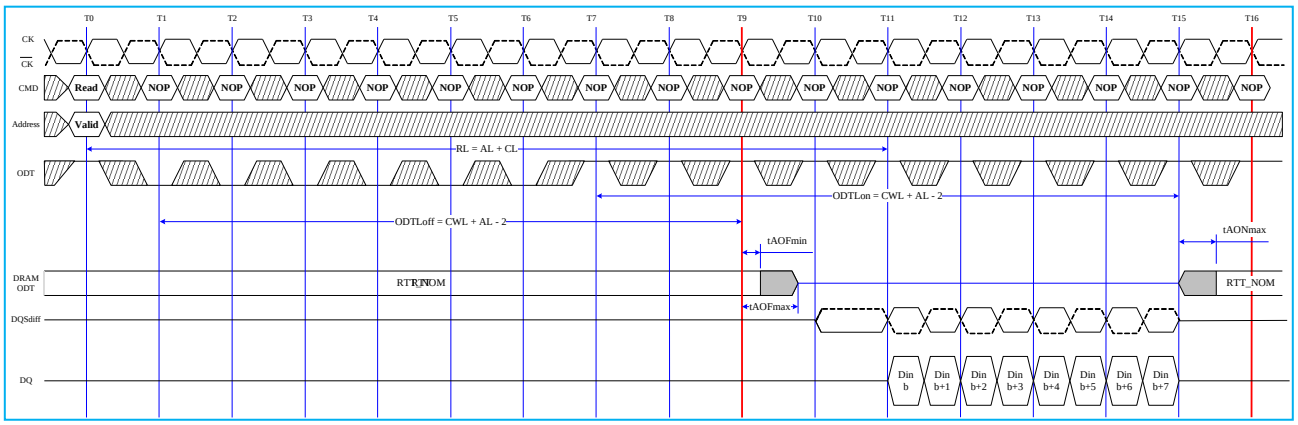



ODT must be held for at least ODTH4 after assertion (T1); ODT must be kept high ODTH4 (BL=4) or ODTH8 (BL=8) after Write command (T7). ODTH is measured from ODT first registered high to ODT first registered low, or from registration of Write command with ODT high to ODT registered low. Note that although ODTH4 is satisfied from ODT registered at T6 ODT must not go low before T11 as ODTH4 must also be satisfied from the registration of the Write command at T7.

## ODT during Reads:

As the DDR3 SDRAM cannot terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may not be enabled until the end of the post-amble as shown in the following figure. DRAM turns on the termination when it stops driving which is determined by tHZ. If DRAM stops driving early (i.e. tHZ is early), then tAONmin time may apply. If DRAM stops driving late (i.e. tHZ is late), then DRAM complies with tAONmax timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example.

**ODT must be disabled externally during Reads by driving ODT low. (Example: CL=6; AL=CL-1=5; RL=AL+CL=11; CWL=5; ODTLon=CWL+AL-2=8; ODTLoff=CWL+AL-2=8)**



## Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

## Functional Description

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to '1'. The function is described as follows:

Two RTT values are available: RTT_Nom and RTT_WR.

The value for RTT_Nom is preselected via bits A[9,6,2] in MR1.

The value for RTT_WR is preselected via bits A[10,9] in MR2.

During operation without write commands, the termination is controlled as follows:

Nominal termination strength RTT_Nom is selected.

Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.

When a Write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:

A latency ODTLcnw after the write command, termination strength RTT_WR is selected.

A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.

Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

The following table shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set RTT_WR, MR2[A10,A9 = [0,0], to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL=4) or ODTH8 (BL=8) after the Write command. ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of Write command until ODT is register low.

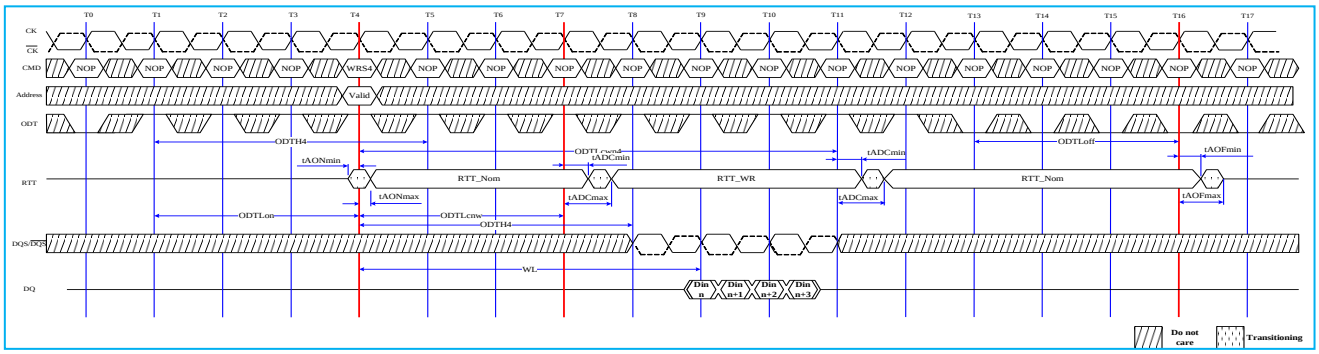
## Latencies and timing parameters relevant for Dynamic ODT

| Name and Description | Abbr. | Defined from | Defined to | Definition for all DDR3 speed pin | Unit |
|---|---|---|---|---|---|
| ODT turn-on Latency | ODTLon | registering external ODT signal high | turning termination on | ODTLon=WL-2 | tCK |
| ODT turn-off Latency | ODTLoff | registering external ODT signal low | turning termination off | ODTLoff=WL-2 | tCK |
| ODT Latency for changing from RTT_Nom to RTT_WR | ODTLcnw | registering external write command | change RTT strength from RTT_Nom to RTT_WR | ODTLcnw=WL-2 | tCK |
| ODT Latency for change from RTT_WR to RTT_Nom (BL=4) | ODTLcwn4 | registering external write command | change RTT strength from RTT_WR to RTT_Nom | ODTLcwn4=4+ODTLoff | tCK |
| ODT Latency for change from RTT_WR to RTT_Nom (BL=8) | ODTLcwn8 | registering external write command | change RTT strength from RTT_WR to RTT_Nom | ODTLcwn8=6+ODTLoff | tCK(avg) |
| Minimum ODT high time after ODT assertion | ODTH4 | registering ODT high | ODT registered low | ODTH4=4 | tCK(avg) |
| Minimum ODT high time after Write (BL=4) | ODTH4 | registering write with ODT high | ODT registered low | ODTH4=4 | tCK(avg) |
| Minimum ODT high time after Write (BL=8) | ODTH8 | registering write with ODT high | ODT register low | ODTH8=6 | tCK(avg) |
| RTT change skew | tADC | ODTLcnw<br>ODTLcwn | RTT valid | tADC(min)=0.3tCK(avg)<br>tADC(max)=0.7tCK(avg) | tCK(avg) |

Note: tAOF,nom and tADC,nom are 0.5tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw, and ODTLcwn)

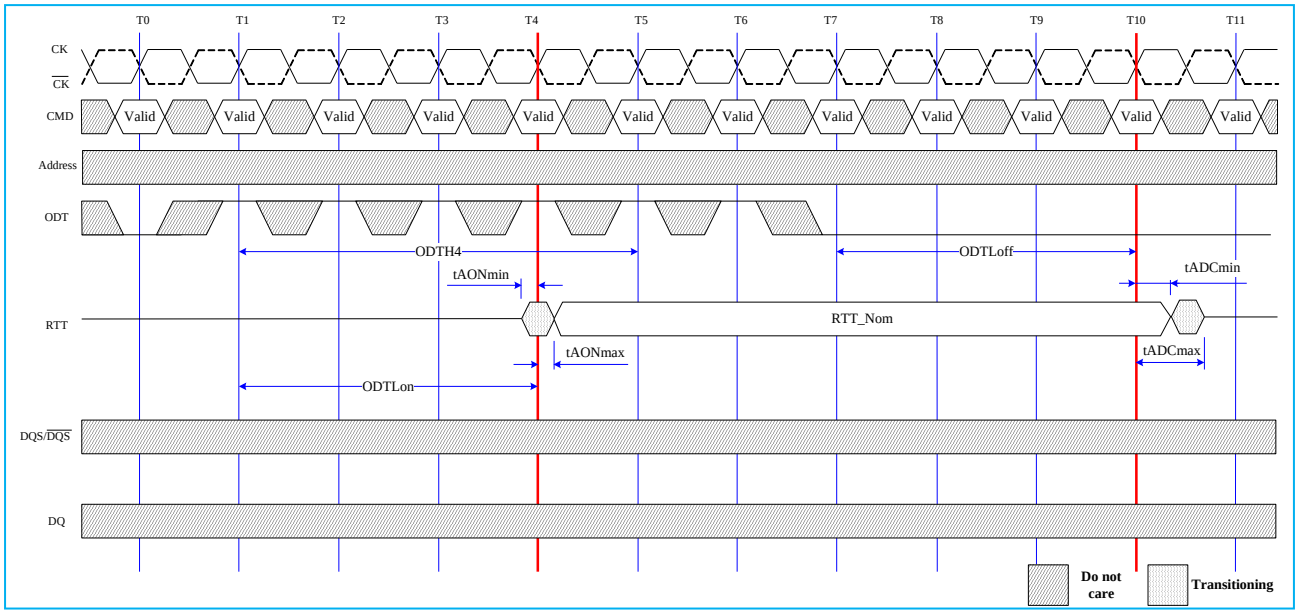
## ODT Timing Diagrams

## Dynamic ODT: Behavior with ODT being asserted before and after the write



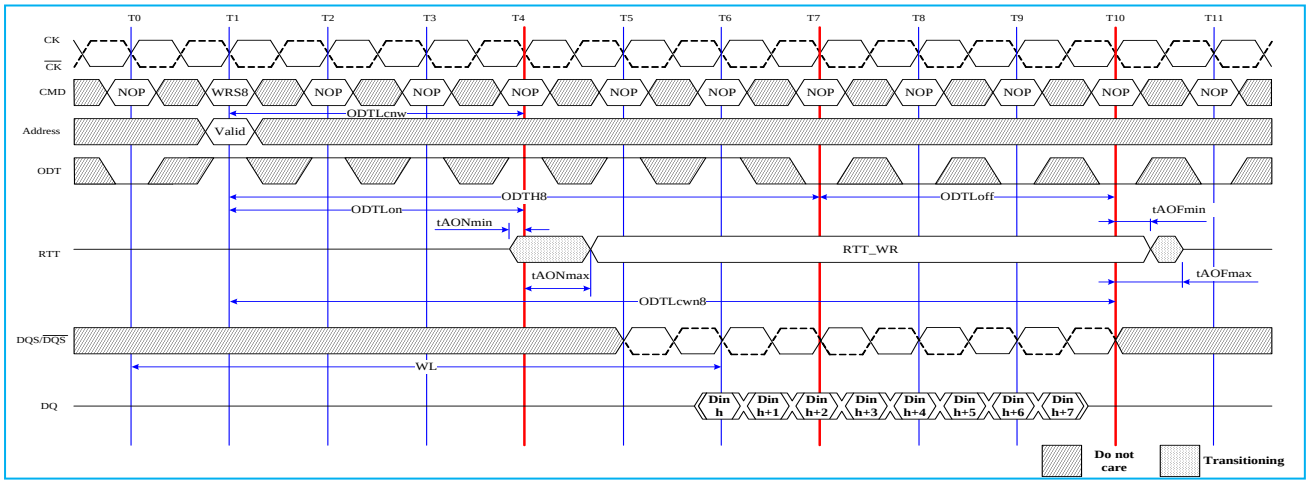

Note: Example for BC4 (via MRS or OTF), AL=0, CWL=5. ODTH4 applies to first registering ODT high and to the registration of the Write command. In this example ODTH4 would be satisfied if ODT went low at T8. (4 clocks after the Write command).

## Dynamic ODT: Behavior without write command, AL=0, CWL=5



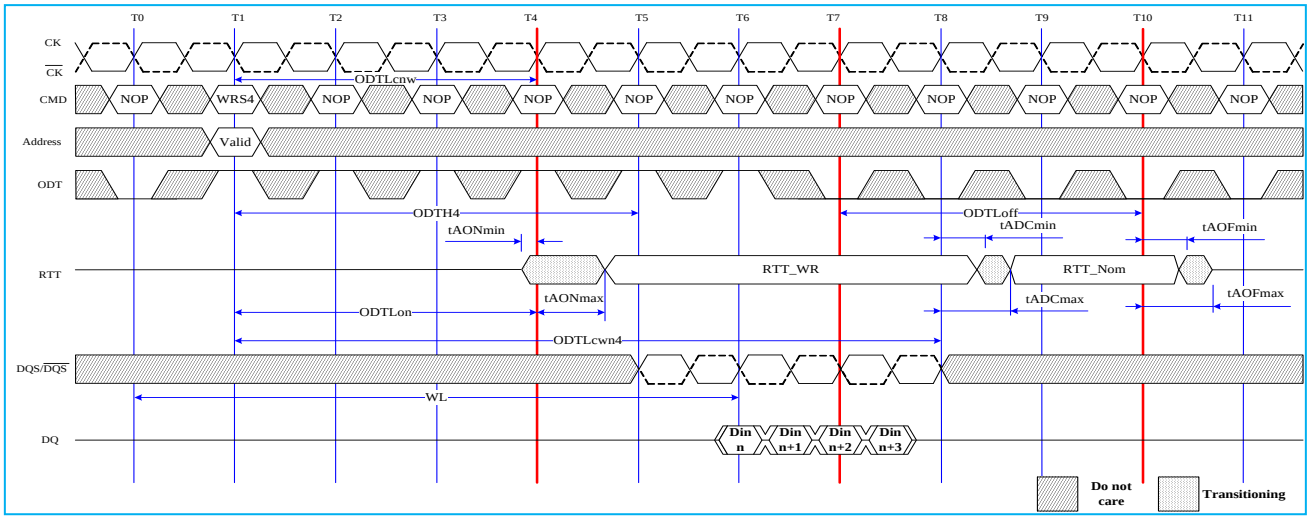

Note: ODTH4 is defined from ODT registered high to ODT registered low, so in this example ODTH4 is satisfied; ODT registered low at T5 would also be legal.

## Dynamic ODT: Behavior with ODT pin being asserted together with write command for the duration of 6 clock cycles.

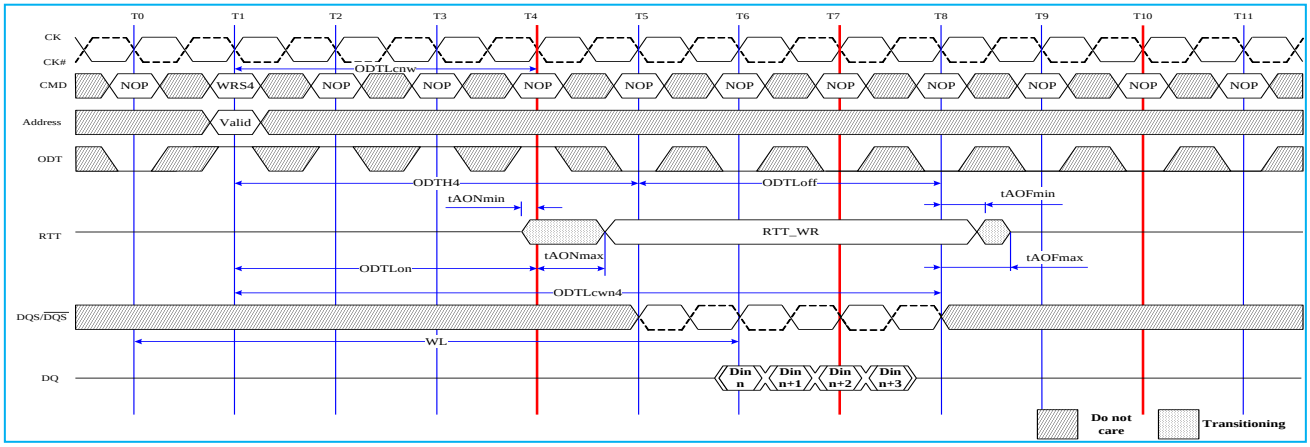



Note: Example for BL8 (via MRS or OTF), AL=0, CWL=5. In this example ODTH8=6 is exactly satisfied.

## Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL=0, CWL=5.




## Dynamic ODT: Behavior with ODT pin being asserted together with write command for the duration of 4 clock cycles.



## Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

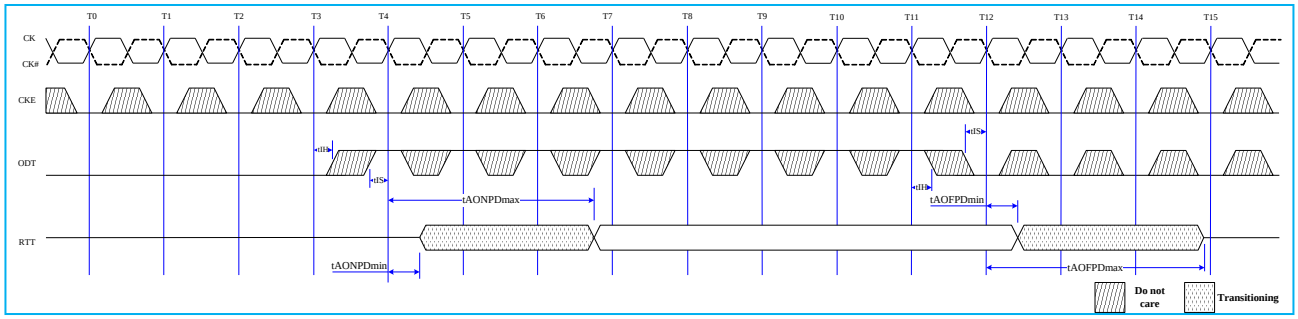
In asynchronous ODT mode, the following timing parameters apply: tAONPD min/max, tAOFPD min/max.

Minimum RTT turn-on time (tAONPD min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time (tAONPD max) is the point in time when the ODT resistance is fully on.

tAONPDmin and tAONPDmax are measured from ODT being sampled high.

Minimum RTT turn-off time (tAOFPDmin) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (tAOFPDmax) is the point in time when the on-die termination has reached high impedance. tAOFPDmin and tAOFPDmax are measured from ODT being sample low.

## Asynchronous ODT Timings on DDR3 SDRAM with fast ODT transition: AL is ignored.




In Precharge Power Down, ODT receiver remains active, however no Read or Write command can be issued, as the respective ADD/CMD receivers may be disabled.

## Asynchronous ODT Timing Parameters for all Speed Bins

| Symbol | Description | min | max | Unit |
|---|---|---|---|---|
| tAONPD | Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | 1 | 9 | ns |
| tAOFPD | Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | 1 | 9 | ns |

## ODT timing parameters for Power Down (with DLL frozen) entry and exit transition period

| Description | min | max |
|---|---|---|
| ODT to RTT turn-on delay | min{ ODTLon * tCK + tAONmin; tAONPDmin }<br>min{ (WL - 2) * tCK + tAONmin; tAONPDmin } | max{ ODTLon * tCK + tAONmax; tAONPDmax }<br>max{ (WL - 2) * tCK + tAONmax; tAONPFmax } |
| ODT to RTT turn-off delay | min{ ODTLoff * tCK + tAOFmin; tAOFPDmin }<br>min{ (WL - 2) * tCK + tAOFmin; tAOFPDmin } | max{ ODTLoff * tCK + tAOFmax; tAOFPDmax }<br>max{ (WL - 2) * tCK + tAOFmax; tAOFPDmax } |
| tANPD | WL-1 | |

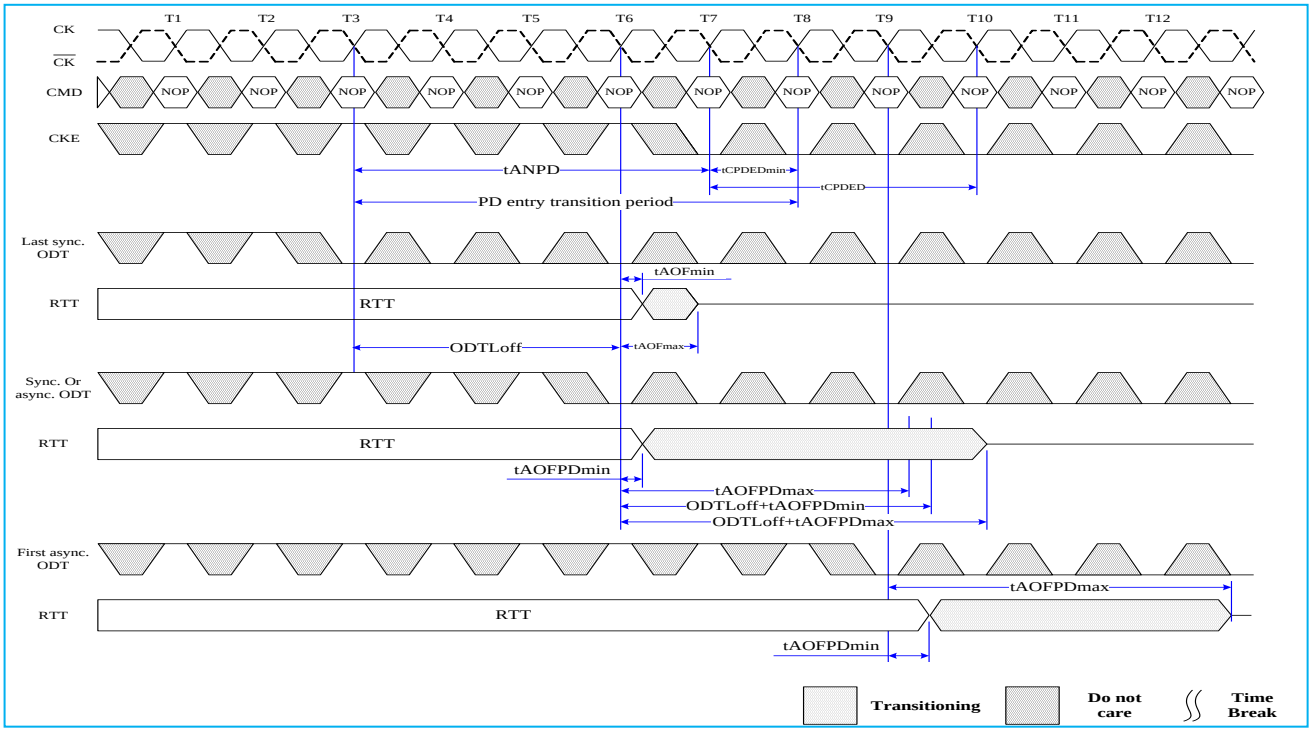
## Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is a transition period around power down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

The transition period is defined by the parameters tANPD and tCPDED(min). tANPD is equal to (WL-1) and is counted backwards in time from the clock cycle where CKE is first registered low. tCPDED(min) starts with the clock cycle where CKE is first registered low. The transition period begins with the starting point of tANPD and terminates at the end point of tCPDED(min). If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of tRFC(min) after the Refresh command and the end point of tCPDED(min). Please note that the actual starting point at tANPD is excluded from the transition period, and the actual end point at tCPDED(min) and tRFC(min, respectively, are included in the transition period.

ODT assertion during the transition period may result in an RTT changes as early as the smaller of tAONPDmin and (ODTLon*tck+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODTLoff*tCK+tAOFmax). Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

## Synchronous to asynchronous transition during Precharge Power Down (with DLL frozen) entry (AL=0; CWL=5; tANPD=WL-1=4)



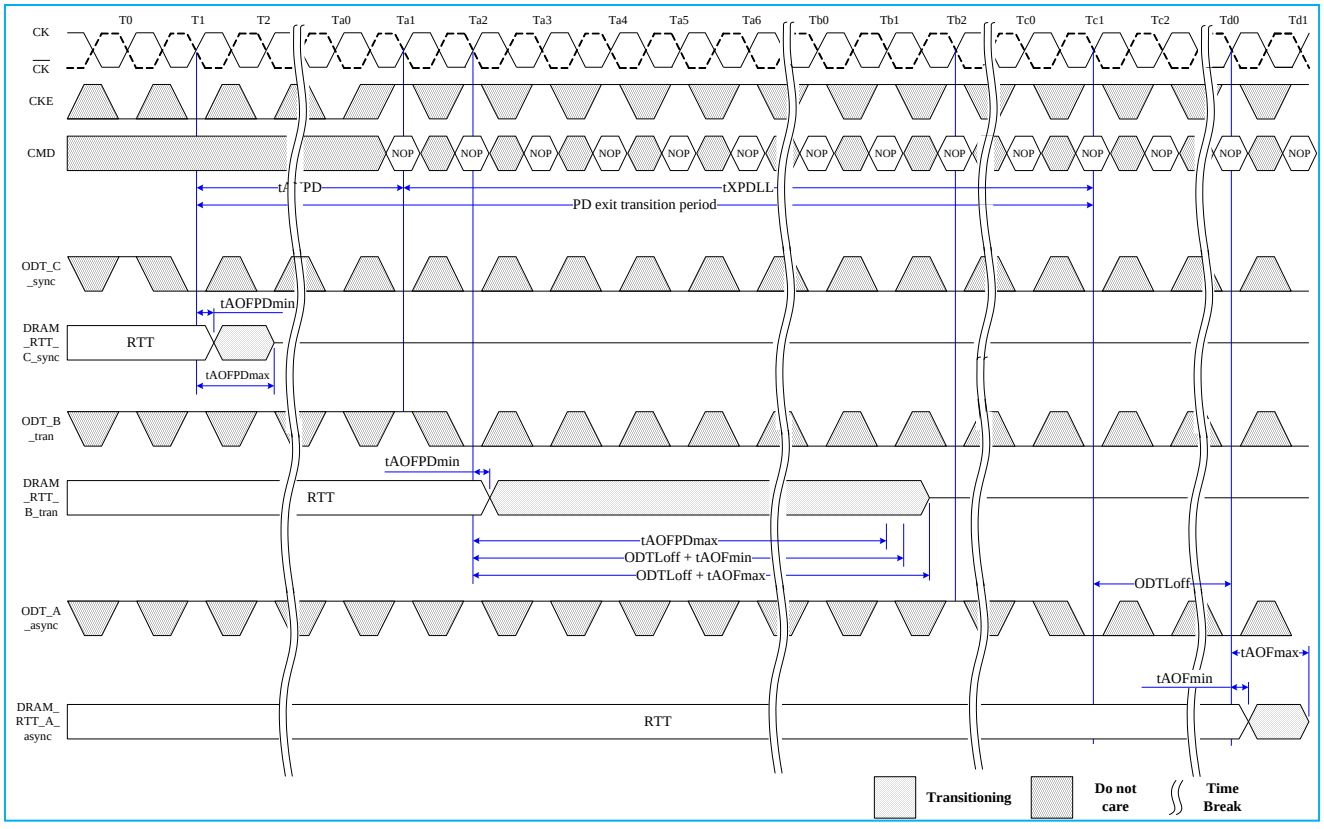
## Asynchronous to Synchronous ODT Mode transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.

This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to (WL -1) and is counted (backwards) from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of tAONPDmin and (ODT-Lon*tCK+tAONmin) and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODToff*tCK+tAOFmax). Note that if AL has a large value, the range where RTT is uncertain becomes quite large. The following figure shows the three different cases: ODT_C, asynchronous response before tANPD; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

## Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL=6; AL=CL-1; CWL=5; tANPD=WL-1=9)

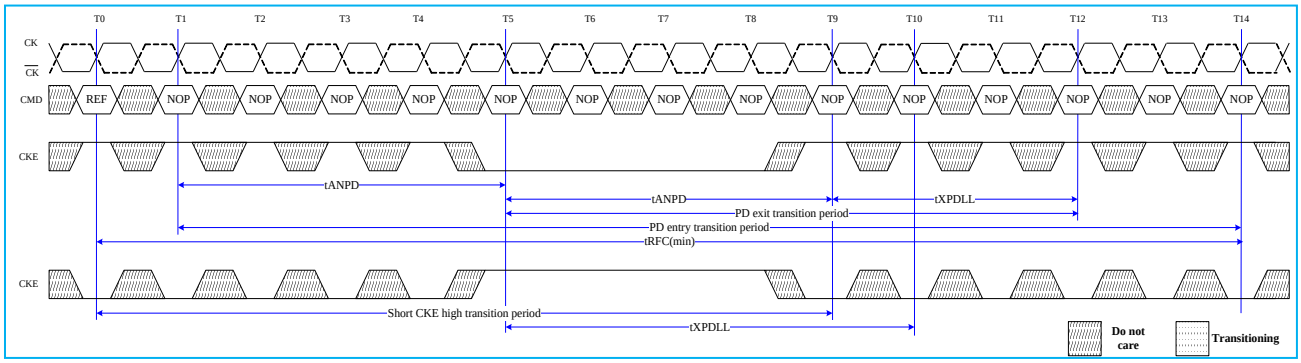


## Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap. In this case, the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous or asynchronous from the state of the PD entry transition period to the end of the PD exit transition period (even if the entry ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD entry may overlap. In this case, the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous or asynchronous from the state of the PD exit transition period to the end of the PD entry transition period. Note that in the following figure, it is assumed that there was no Refresh command in progress when Idle state was entered.

## Transition period for short CKE cycles with entry and exit period overlapping (AL=0; WL=5; tANPD=WL-1=4)



## ZQ Calibration Commands

## ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron and ODT values. DDR3 SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calibrated values are transferred from calibration engine to DRAM IO which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS.

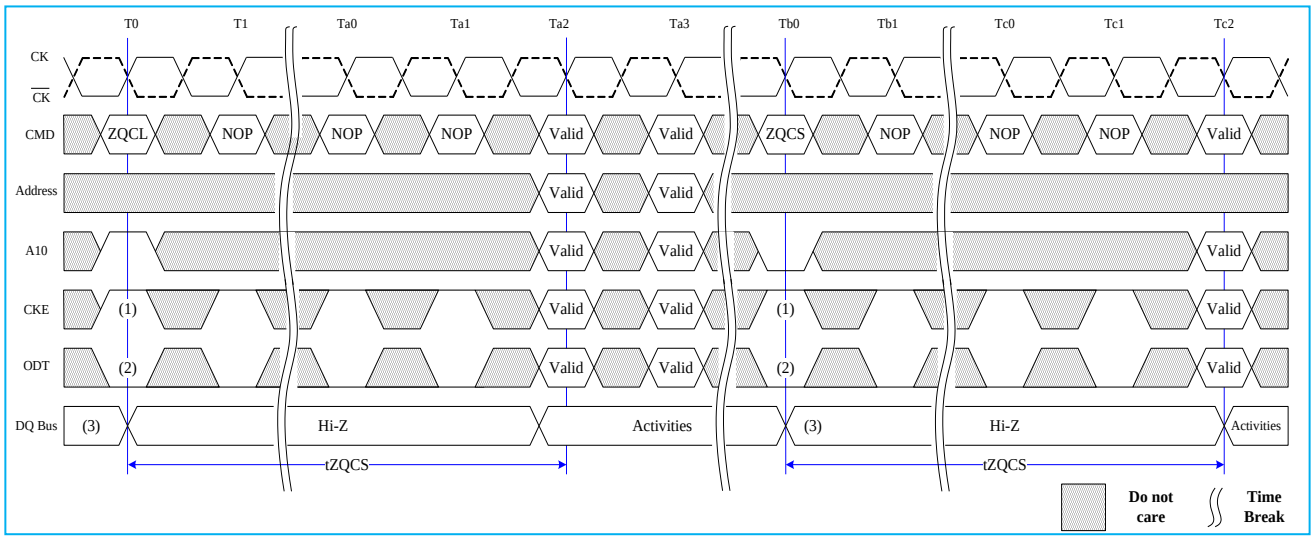
No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon self-refresh exit, DDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between ranks.

## ZQ Calibration Timing




Note:

1. CKE must be continuously registered high during the calibration procedure.

2. On-die termination must be disabled via the ODT signal or MRS during the calibration procedure.

3. All devices connected to the DQ bus should be high impedance during the calibration procedure.

## ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ calibration function, a 240 ohm +/- 1% tolerance external resistor connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited.

## Absolute Maximum Ratings

### Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Note |
|---|---|---|---|---|
| VDD | Voltage on VDD pin relative to Vss | -0.4 ~ 1.975 | V | 1,3 |
| VDDQ | Voltage on VDDQ pin relative to Vss | -0.4 ~ 1.975 | V | 1,3 |
| Vin, Vout | Voltage on any pin relative to Vss | -0.4 ~ 1.975 | V | 1 |
| Tstg | Storage Temperature | -55 ~ 100 | °C | 1,2 |

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and Vref must be not greater than 0.6VDDQ, when VDD and VDDQ are less than 500mV; Vref may be equal to or less than 300mV.

## Temperature Range

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| Toper | Normal Operating Temperature Range | 0 to 85 | °C | 1,2 |
| | Extended Temperature Range | 85 to 95 | °C | 1,3 |

Note:

1. Operating Temperature Toper is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional apply:

a) Refresh commands must be doubled in frequency, therefore, reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1x refresh (tREFI to 7.8us) in the Extended Temperature Range.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0 and MR2 A7=1) or enable the optional Auto Self-Refresh mode (MR2 A6=1 and MR2 A7=0).

## AC & DC Operating Conditions

## Recommended DC Operating Conditions

| Symbol | Parameter | Rating | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1,2 |
| VDDQ | Supply Voltage for Output | 1.425 | 1.5 | 1.575 | V | 1,2 |
| VDD | Supply Voltage | 1.28 | 1.35 | 1.45 | V | 1,2 |
| VDDQ | Supply Voltage for Output | 1.28 | 1.35 | 1.45 | V | 1,2 |

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.

2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

## AC & DC Input Measurement Levels

## AC and DC Logic Input Levels for Single-Ended Signals & Command and Address

| Symbol | Parameter | DDR3-800/1066/1333/1600 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| VIH.CA(DC100) | DC input logic high | Vref + 0.100 | VDD | V | 1 |
| VIL.CA(DC100) | DC input logic low | VSS | Vref - 0.100 | V | 1 |
| VIH.CA(AC175) | AC input logic high | Vref + 0.175 | Note2 | V | 1,2 |
| VIL.CA(AC175) | AC input logic low | Note2 | Vref - 0.175 | V | 1,2 |
| VIH.CA(AC150) | AC input logic high | Vref + 0.150 | Note2 | V | 1,2 |
| VIL.CA(AC150) | AC input logic low | Note2 | Vref - 0.150 | V | 1,2 |
| VREFCA(DC) | Reference Voltage for ADD, CMD inputs | 0.49 * VDD | 0.51 * VDD | V | 3,4 |

Note:

1. For input only pins except RESET.Vref=VrefCA(DC)

2. See "Overshoot and Undershoot Specifications"

3. The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than +/- 0.1% VDD.

4. For reference: approx. VDD/2 +/- 15mV.

5. To allow VREFCA margining, all DRAM Command and Address Input Buffers MUST use external VREF (provided by system) as the input for their VREFCA pins. All VIH/L input level MUST be compared with the external VREF level at the 1st stage of the Command and Address input buffer

## AC and DC Logic Input Levels for Single-Ended Signals & DQ and DM

| Symbol | Parameter | DDR3-800/1066 | | DDR3-1333/1600 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| VIH.DQ(DC100) | DC input logic high | Vref + 0.100 | VDD | Vref + 0.100 | VDD | V | 1 |
| VIL.DQ(DC100) | DC input logic low | VSS | Vref - 0.100 | VSS | Vref - 0.100 | V | 1 |
| VIH.DQ(AC175) | AC input logic high | Vref + 0.175 | Note2 | Vref + 0.150 | Note2 | V | 1,2,5 |
| VIL.DQ(AC175) | AC input logic low | Note2 | Vref - 0.175 | Note2 | Vref - 0.150 | V | 1,2,5 |
| VIH.DQ(AC150) | AC input logic high | Vref + 0.150 | Note2 | Vref + 0.150 | Note2 | V | 1,2,5 |
| VIL.DQ(AC150) | AC input logic low | Note2 | Vref - 0.150 | Note2 | Vref - 0.150 | V | 1,2,5 |
| VREFDQ(DC) | Reference Voltage for DQ, DM inputs | 0.49 * VDD | 0.51 * VDD | 0.49 * VDD | 0.51 * VDD | V | 3,4 |
| VREFDQ_t(DC) | Reference Voltage for trained DQ, DM inputs | **0.45 * VDD** | **0.55 * VDD** | **0.45 * VDD** | **0.55 * VDD** | **V** | **3,4 6,7** |

Note:

1. For input only pins except $\overline{\text{RESET}}$. Vref = VrefDQ(DC)
2. See "Overshoot and Undershoot Specifications"
3. The ac peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than ± 0.1% VDD.
4. For reference: approx. VDD/2 ±15mV.
5. Single-ended swing requirement for DQS-$\overline{\text{DQS}}$, is 350mV (peak to peak). Differential swing requirement for DQS-$\overline{\text{DQS}}$, is 700mV (peak to peak)
6. VRefDQ training is performed only during system boot. Once the training is completed and an optimal VRefDQ_t(DC) voltage level is identified, the optimal VRefDQ_t(DC) voltage level will be used during system runtime. During VRefDQ training, VRefDQ is swept from 40% of VDD to 60% of VDD to find the optimal VRefDQ_t(DC) voltage level; and once the optimal VRefDQ_t(DC) is set, it must stay within +/- 1% of its set value as well as not be less than 45% of VDD or exceed 55% of VDD. VIH.DQ(AC)min/VIL.DQ(AC)max = Optimal VRefDQ_t(DC) +/- AC Level, where "AC Level" is the actual AC voltage level per DDR3 speed bins as specified in JESD79-3 specification. After VRefDQ training is completed and the optimal VRefDQ_t(DC) is set, the Memory Controller provides the DRAM device a valid write window. Through DQS placement optimization and VRefDQ centering, the valid write window is optimized for both input voltage margin and tDS+tDH window for the DRAM receiver. The DRAM device supports the use of the above techniques to optimize the write timing and voltage margin, as long as the technique does not create any DIMM failures due to DRAM input voltage and/or timing spec violations as defined in JESD79-3 specification.
7. To allow VREFDQ margining, all DRAM Data Input Buffers MUST use external VREF (provided by system) as the input for their VREFDQ pins. All VIH/L input level MUST be compared with the external VREF level at the 1st stage of the Data input buffer.

## AC and DC Output Measurement Levels

### Single Ended AC and DC Output Levels

| Symbol | Parameter | Value | Unit | Notes |
|---|---|---|---|---|
| VOH(DC) | DC output high measurement level (for IV curve linearity) | 0.8xVDDQ | V | |
| VOM(DC) | DC output mid measurement level (for IV curve linearity) | 0.5xVDDQ | V | |
| VOL(DC) | DC output low measurement level (fro IV curve linearity) | 0.2xVDDQ | V | |
| VOH(AC) | AC output high measurement level (for output SR) | VTT+0.1xVDDQ | V | 1 |
| VOL(AC) | AC output low measurement level (for output SR) | VTT-0.1xVDDQ | V | 1 |

Note:

1. The swing of ±0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2.

### Differential AC and DC Output Levels

| Symbol | Parameter | DDR3 | Unit | Notes |
|---|---|---|---|---|
| VOHdiff(AC) | AC differential output high measurement level (for output SR) | +0.2 x VDDQ | V | 1 |
| VOLdiff(AC) | AC differential output low measurement level (for output SR) | -0.2 x VDDQ | V | 1 |

Note:

1. The swing of ± 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT=VDDQ/2 at each of the differential outputs.

## ODT DC Electrical Characteristics, assuming $R_{ZQ}$ = 240ohms +/- 1% entire operating temperature range; after proper ZQ calibration

| MR1 A9, A6, A2 | RTT | Resistor | Vout | min | nom | max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| 0,1,0 | 120Ω | $RTT_{120Pd240}$ | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | $R_{ZQ}$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}$ | 1,2,3,4 |
| | | $RTT_{120Pu240}$ | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1,1 | $R_{ZQ}$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}$ | 1,2,3,4 |
| | | $RTT_{120}$ | VIL(ac) to VIH(ac) | 0.9 | 1 | 1.6 | $R_{ZQ}$ /2 | 1,2,5 |
| 0, 0, 1 | 60Ω | $RTT_{60Pd120}$ | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}/2$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | $R_{ZQ}/2$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}/2$ | 1,2,3,4 |
| | | $RTT_{60Pu120}$ | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}/2$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | $R_{ZQ}/2$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}/2$ | 1,2,3,4 |
| | | $RTT_{60}$ | VIL(ac) to VIH(ac) | 0.9 | 1 | 1.6 | $R_{ZQ}/4$ | 1,2,5 |
| 0, 1, 1 | 40Ω | $RTT_{40Pd80}$ | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}/3$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | $R_{ZQ}/3$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}/3$ | 1,2,3,4 |
| | | RTT40Pu80 | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}/3$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | $R_{ZQ}/3$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}/3$ | 1,2,3,4 |
| | | RTT40 | VIL(ac) to VIH(ac) | 0.9 | 1 | 1.6 | $R_{ZQ}/6$ | 1,2,5 |
| 1, 0, 1 | 30Ω | RTT30Pd60 | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}/4$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | $R_{ZQ}/4$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}/4$ | 1,2,3,4 |
| | | RTT30Pu60 | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}/4$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | $R_{ZQ}/4$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}/4$ | 1,2,3,4 |
| | | RTT30 | VIL(ac) to VIH(ac) | 0.9 | 1 | 1.6 | $R_{ZQ}/8$ | 1,2,5 |
| 1, 0, 0 | 20Ω | RTT20Pd40 | VOLdc = 0.2 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}/6$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | $R_{ZQ}/6$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}/6$ | 1,2,3,4 |
| | | RTT20Pu40 | VOLdc = 0.2 x VDDQ | 0.9 | 1 | 1.4 | $R_{ZQ}/6$ | 1,2,3,4 |
| | | | 0.5 x VDDQ | 0.9 | 1 | 1.1 | $R_{ZQ}/6$ | 1,2,3,4 |
| | | | VOHdc = 0.8 x VDDQ | 0.6 | 1 | 1.1 | $R_{ZQ}/6$ | 1,2,3,4 |
| | | RTT20 | VIL(ac) to VIH(ac) | 0.9 | 1 | 1.6 | $R_{ZQ}/12$ | 1,2,5 |
| Deviation of VM w.r.t. VDDQ/2, DVm | | | | -5 | | +5 | % | 1,2,5,6 |

Note:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration may be used to achieve the linearity spec shown above.
4. Not a specification requirement, but a design guide line.
5. Measurement definition for RTT:
Apply VIH(ac) to pin under test and measure current / (VIH(ac)), then apply VIL(ac) to pin under test and measure current / (VIL(ac)) respectively.
RTT = [VIH(ac) - VIL(ac)] / [I(VIH(ac)) - I(VIL(ac))]
6. Measurement definition for $V_M$ and $DV_M$:
Measure voltage ($V_M$) at test pin (midpoint) with no lead:
Delta $V_M$ = [2$V_M$ / VDDQ -1] x 100

## ODT Temperature and Voltage sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table.

Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ

## ODT Sensitivity Definition

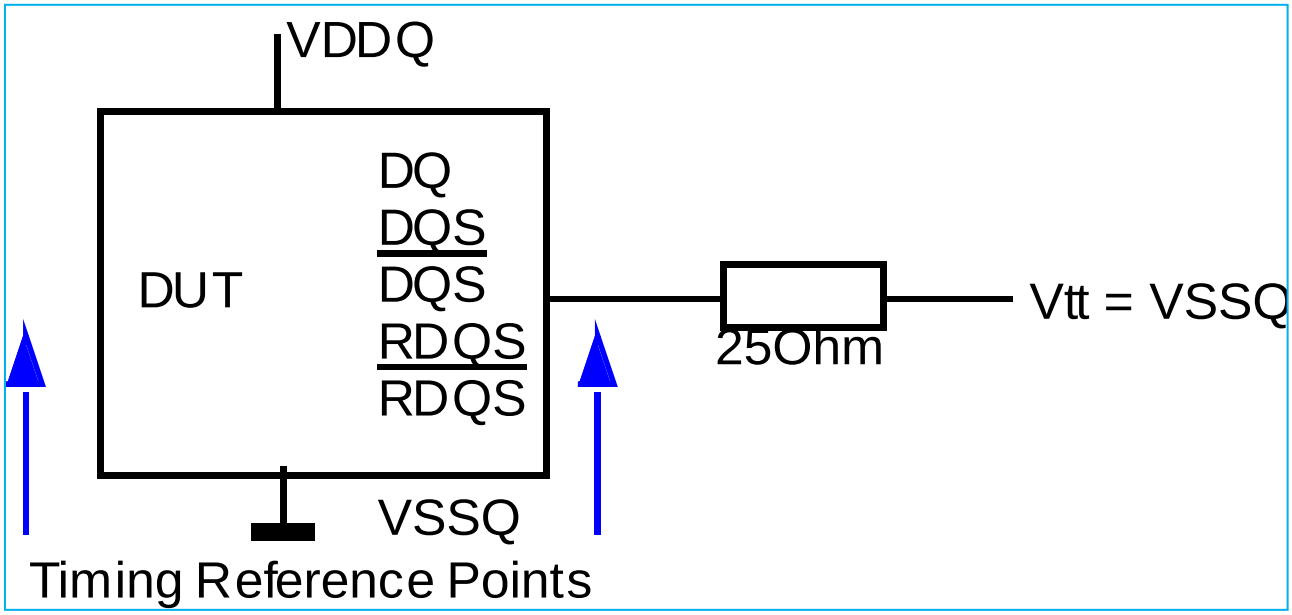
| | min | max | Unit |
|---|---|---|---|
| RTT | 0.9 - dRTTdT*lDelta Tl - dRTTdV*lDelta Vl | 1.6 + dRTTdT*lDelta Tl + dRTTdV*lDelta Vl | RZQ/2,4,6,8,12 |

## ODT Voltage and Temperature Sensitivity

| | min | max | Unit |
|---|---|---|---|
| dRTTdT | 0 | 1.5 | %/°C |
| dRTTdV | 0 | 0.15 | %/mV |
| Note: These parameters may not be subject to production test. They are verified by design and characterization. | | | |

## Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in the following figure.




## ODT Timing Definitions

Definitions for $t_{AON}$, $t_{AONPD}$, $t_{AOF}$, $t_{AOFPD}$, and $t_{ADC}$ are provided in the following table and subsequent figures.

| Symbol | Begin Point Definition | End Point Definition |
|---|---|---|
| tAON | Rising edge of CK - CK defined by the end point of ODTLon | Extrapolated point at VSSQ |
| tAONPD | Rising edge of CK - CK with ODT being first registered high | Extrapolated point at VSSQ |
| tAOF | Rising edge of CK - CK defined by the end point of ODTLoff | End point: Extrapolated point at VRTT_Nom |
| tAOFPD | Rising edge of CK - CK with ODT being first registered low | End point: Extrapolated point at VRTT_Nom |
| tADC | Rising edge of CK - CK defined by the end point of ODTLcnw, ODTLcwn4, or ODTLcwn8 | End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively |

## Reference Settings for ODT Timing Measurements

| Measured Parameter | RTT_Nom Setting | RTT_Wr Setting | VSW1[V] | VSW2[V] | Note |
|---|---|---|---|---|---|
| tAON | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tAONPD | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tAOF | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tAOFPD | RZQ/4 | NA | 0.05 | 0.10 | |
| | RZQ/12 | NA | 0.10 | 0.20 | |
| tADC | RZQ/12 | RZQ/2 | 0.20 | 0.30 | |

### Input / Output Capacitance

| Symbol | Parameter | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max | Min. | Max | Min. | Max | Min. | Max | | |
| $C_{IO}$ | Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$) | 1.50 | 3.00 | 1.50 | 3.00 | 1.50 | 2.50 | 1.50 | 2.30 | pF | 1,2,3 |
| $C_{CK}$ | Input capacitance, CK and CK | 0.80 | 1.60 | 0.80 | 1.60 | 0.80 | 1.40 | 0.80 | 1.40 | pF | 2,3 |
| $C_{DCK}$ | Input capacitance delta, CK and $\overline{CK}$ | 0.00 | 0.15 | 0.00 | 0.15 | 0.00 | 0.15 | 0.00 | 0.15 | pF | 2,3,4 |
| $C_{DDQS}$ | Input/output capacitance delta, DQS and $\overline{DQS}$ | 0.00 | 0.20 | 0.00 | 0.20 | 0.00 | 0.15 | 0.00 | 0.15 | pF | 2,3,5 |
| $C_{I}$ | Input capacitance, CTRL, ADD, CMD input-only pins | 0.75 | 1.40 | 0.75 | 1.35 | 0.75 | 1.30 | 0.75 | 1.30 | pF | 2,3,7,8 |
| $C_{DI\_CTRL}$ | Input capacitance delta, all CTRL input-only pins | -0.50 | 0.30 | -0.50 | 0.30 | -0.40 | 0.20 | -0.40 | 0.20 | pF | 2,3,7,8 |
| $C_{DI\_ADD\_CMD}$ | Input capacitance delta, all ADD/CMD input-only pins | -0.50 | 0.50 | -0.50 | 0.50 | -0.40 | 0.40 | -0.40 | 0.40 | pF | 2,3,9,10 |
| $C_{DIO}$ | Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$ | -0.50 | 0.30 | -0.50 | 0.30 | -0.50 | 0.30 | -0.50 | 0.30 | pF | 2,3,11 |
| $C_{ZQ}$ | Input/output capacitance of ZQ pin | - | 3.00 | - | 3.00 | - | 3.00 | - | 3.00 | pF | 2,3,12 |

1. Although the DM, TDQS and TDQS pins have different functions, the loading matches DQ and DQS
2. This parameter is not subject to production test. It is verified by design and characterization. VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of CCK-CCK
5. Absolute value of CIO(DQS)-CIO(DQS)
6. CI applies to ODT, $\overline{CS}$, CKE, A0-A13, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
7. CDI_CTRL applies to ODT, $\overline{CS}$ and CKE
8. CDI_CTRL=CI(CTRL)-0.5*(CI(CLK)+CI(CLK))
9. CDI_ADD_CMD applies to A0-A13, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$
10. CDI_ADD_CMD=CI(ADD_CMD) - 0.5*(CI(CLK)+CI($\overline{CLK}$))
11. CDIO=CIO(DQ,DM) - 0.5*(CIO(DQS)+CIO($\overline{DQS}$))
12. Maximum external load capacitance on ZQ pin: 5 pF.

## IDD Specifications and Measurement Conditions

| Symbol | Parameter/Condition | DDR3-800MHz | | | DDR3-1066MHz | | | DDR3-1333MHz | | | DDR3-1600MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | X4 | X8 | X16 | X4 | X8 | X16 | X4 | X8 | X16 | X4 | X8 | X16 | |
| IDD0 | Operating Current 0<br>-> One Bank Activate<br>-> Precharge | 70 | 70 | 80 | 75 | 75 | 90 | 85 | 85 | 100 | 95 | 95 | 110 | mA |
| IDD1 | Operating Current 1<br>-> One Bank Activate<br>-> Read<br>-> Precharge | 90 | 90 | 120 | 95 | 95 | 125 | 100 | 100 | 130 | 105 | 105 | 135 | mA |
| IDD2P0 | Precharge Power-Down Current<br>Slow Exit - MR0 bit A12 = 0 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | mA |
| IDD2P1 | Precharge Power-Down Current<br>Fast Exit - MR0 bit A12 = 1 | 20 | 20 | 25 | 25 | 25 | 30 | 30 | 30 | 35 | 35 | 35 | 40 | mA |
| IDD2Q | Precharge Quiet Standby Current | 25 | 25 | 25 | 30 | 30 | 30 | 35 | 35 | 35 | 40 | 40 | 40 | mA |
| IDD2N | Precharge Standby Current | 30 | 30 | 30 | 35 | 35 | 35 | 40 | 40 | 40 | 45 | 45 | 45 | mA |
| IDD3P | Active Power-Down Current<br>Always Fast Exit | 25 | 25 | 30 | 30 | 30 | 35 | 35 | 35 | 40 | 40 | 40 | 45 | mA |
| IDD3N | Active Standby Current | 30 | 30 | 30 | 35 | 35 | 35 | 40 | 40 | 40 | 45 | 45 | 45 | mA |
| IDD4R | Operating Current Burst Read | 120 | 120 | 180 | 140 | 140 | 210 | 160 | 160 | 240 | 180 | 180 | 270 | mA |
| IDD4W | Operating Current Burst Write | 125 | 125 | 190 | 145 | 145 | 210 | 165 | 165 | 255 | 185 | 185 | 280 | mA |
| IDD5B | Burst Refresh Current | 180 | 180 | 180 | 190 | 190 | 190 | 200 | 200 | 200 | 210 | 210 | 210 | mA |
| IDD6 | Self-Refresh Current Normal Temperature Range (0-85°C) | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | mA |
| IDD7 | All Bank Interleave Read Current | 280 | 280 | 300 | 310 | 310 | 330 | 330 | 330 | 370 | 370 | 370 | 400 | mA |

| Symbol | Parameter/Condition | DDR3-800MHz | | | DDR3-1066MHz | | | DDR3-1333MHz | | | DDR3-1600MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | X4 | X8 | X16 | X4 | X8 | X16 | X4 | X8 | X16 | X4 | X8 | X16 | |
| IDD0 | Operating Current 0<br>-> One Bank Activate<br>-> Precharge | 65 | 65 | 73 | 69 | 69 | 83 | 78 | 78 | 92 | 87 | 87 | 100 | mA |
| IDD1 | Operating Current 1<br>-> One Bank Activate<br>-> Read<br>-> Precharge | 83 | 83 | 110 | 87 | 87 | 115 | 92 | 92 | 120 | 96 | 96 | 124 | mA |
| IDD2P0 | Precharge Power-Down Current<br>Slow Exit - MR0 bit A12 = 0 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | mA |
| IDD2P1 | Precharge Power-Down Current<br>Fast Exit - MR0 bit A12 = 1 | 18.5 | 18.5 | 23 | 23 | 23 | 27.5 | 27.5 | 27.5 | 32 | 32 | 32 | 36.5 | mA |
| IDD2Q | Precharge Quiet Standby Current | 23 | 23 | 23 | 27.5 | 27.5 | 27.5 | 32 | 32 | 32 | 36.5 | 36.5 | 36.5 | mA |
| IDD2N | Precharge Standby Current | 27.5 | 27.5 | 27.5 | 32 | 32 | 32 | 36.5 | 36.5 | 36.5 | 41.5 | 41.5 | 41.5 | mA |
| IDD3P | Active Power-Down Current<br>Always Fast Exit | 23 | 23 | 27.5 | 27.5 | 27.5 | 32 | 32 | 32 | 36.5 | 36.5 | 36.5 | 41.5 | mA |
| IDD3N | Active Standby Current | 27.5 | 27.5 | 27.5 | 32 | 32 | 32 | 36.5 | 36.5 | 36.5 | 41.5 | 41.5 | 41.5 | mA |
| IDD4R | Operating Current Burst Read | 110 | 110 | 165 | 130 | 130 | 190 | 147 | 147 | 220 | 165 | 165 | 247.5 | mA |
| IDD4W | Operating Current Burst Write | 115 | 115 | 175 | 130 | 130 | 190 | 150 | 150 | 235 | 170 | 170 | 255 | mA |
| IDD5B | Burst Refresh Current | 165 | 165 | 165 | 175 | 175 | 175 | 185 | 185 | 185 | 190 | 190 | 190 | mA |
| IDD6 | Self-Refresh Current Normal Temperature Range (0-85°C) | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | mA |
| IDD7 | All Bank Interleave Read Current | 250 | 250 | 270 | 280 | 280 | 300 | 300 | 300 | 340 | 330 | 330 | 370 | mA |

## IDD Measurement Conditions

| Symbol | Parameter/Condition |
|---|---|
| IDD0 | Operating Current - One bank Active - Precharge current<br>CKE: High; External clock: On; tCK, tRC, tRAS: see table in the next page; CS: High between ACT and PRE; Command Inputs: SWITCHING[1] (except for ACT and PRE); Row, Column Address, Data I/O: SWITCHING1 (A10 Low permanently); Bank Address: fixed (Bank 0); Output Buffer: off [2]; ODT: disabled [3]; Active Banks: one (ACT-PRE loop); Idle Banks: all other; Pattern example: A0 D DD DD DD DD DD DD D P0[4] (DDR3-800: tRAS=37.5ns) |
| IDD1 | Operating One bank Active-Read-Precharge Current<br>CKE: High; External clock: On; tCK, tRC, tRAS, tRCD, CL, AL: see table in the next page; CS: High between ACT, RD, and PRE; Command Inputs: SWITCHING[1] (except ACT, RD, and PRE Commands); Row, Column Address: SWITCHING1 (A10 Low permanently); Bank Address: fixed (Bank 0); Data I/O: switching every clock (RD Data stable during one Clock cycle); floating when no burst activity; Output Buffer: Off[2]; ODT: disabled [3]; Burst Length: BL85; Active Banks: one (ACT-RD-PRE loop); Idle Banks: all other; Pattern example: A0 D DD D R0 DD DD DD DD DD D P0[4] (DDR3-800-5-5-5: tRCD=12.5ns). |
| IDD2N | Precharge Standby Current<br>CKE=High; External Clock=On; tCK: see table in the next page; CS: High; Command Inputs, Row, Column, Bank Address, Data I/O: SWITCHING[1] ; Output Buffer: Off[2]; ODT: disabled [3]; Active / Idle Banks: none / all. |
| IDD2P(0) | Precharge Power-Down Current - (Slow Exit)<br>CKE=Low; External Clock=On; tCK: see table in the next page; CS: Stable; Command Inputs: Stable; Row, Column / Bank Address: Stable; Data I/O: floating; Output Buffer: Off[2]; ODT: disabled [3]; Active / Idle Banks: none / all. Precharge Power Down Mode: Slow Exit [6](RD and ODT must satisfy tXPDLL - AL) |
| IDD2P(1) | Precharge Power-Down Current - (Fast Exit)<br>CKE=Low; External Clock=On; tCK: see table in the next page; CS: Stable; Command Inputs, Row, Column, Bank Address: Stable; Data I/O: floating; Output Buffer: Off[2]; ODT: disabled [3]; Active / Idle Banks: none / all. Precharge Power Down Mode: Fast Exit 6(any valid Command after tXP)[7] |
| IDD2Q | Precharge Quiet Standby Current<br>CKE=High; External Clock=On; tCK: see table in the next page; CS=High; Command Inputs, Row, Column, Bank Address: Stable; Data I/O: floating; Output Buffer: Off2; ODT: disabled [3]; Active / Idle Banks: none / all. |
| IDD3N | Active Standby Current<br>CKE=High; External Clock=On; tCK: see table in the next page; CS=High; Command Inputs, Row, Column, Bank Address, Data I/O: SWITCHING[1]; Output Buffer: Off2; ODT: disabled [3]; Active / Idle Banks: All / none. |
| IDD3P | Active Power-Down Current<br>CKE=Low; External Clock=On; tCK: see table in the next page; CS, Command Inputs, Row, Column, Bank Address: Stable; Data I/O: floating; Output Buffer: Off2; ODT: disabled [3]; Active / Idle Banks: All / none. |
| IDD4R | Operating Burst Read Current<br>CKE=High; External Clock=On; tCK, CL: see table in the next page; AL: 0; CS: High between valid Commands; Command Inputs: SWITCHING[1](except RD Commands); Row, Column Address: SWITCHING[1](A10: Low permanently); Bank Address: cycling[10]; Data I/O: Seamless Read Data Burst : Output Data switches every clock cycle (i.e. data stable during one clock cycle); Output Buffer: Off[2]; ODT: disabled [3]; Burst Length: BL8[5]; Active / Idle Banks: All / none[10]; Pattern: R0 D DD R1 D DD R2 D DD R3 D DD R4[4] |
| IDD4W | Operating Burst Write Current<br>CKE=High; External Clock=On; tCK, CL: see table in the next page; AL: 0; CS: High between valid Commands; Command Inputs: SWITCHING[1](except WR Commands); Row, Column Address: SWITCHING[1](A10: Low permanently); Bank Address: cycling[10]; Data I/O: Seamless Write Data Burst : Input Data switches every clock cycle (i.e. data stable during one clock cycle); DM: L permanently; Output Buffer: Off[2]; ODT: disabled [3]; Burst Length: BL8[5]; Active / Idle Banks: All / none[10]; Pattern: W0 D DD W1 D DD W2 D DD W3 D DD W4[4] |
| IDD5B | Burst Refresh Current<br>CKE=High; External Clock=On; tCK, tRFC: see table in the next page; CS: High between valid Commands; Command Inputs, Row, Column, Bank Addresses, Data I/O: SWITCHING[1]; Output Buffer: Off[2]; ODT: disabled [3]; Active Banks: Refresh Command every tRFC=tRFC(IDD); Idle banks: none. |
| IDD6 | Self-Refresh Current<br>Tcase=0-85°C; Auto Self Refresh =Disable; Self Refresh Temperature Range=Normal[9]; CKE=Low; External Clock=Off (CK and CK: Low); CS, Command Inputs, Row, Column Address, Bank Address, Data I/O: Floating; Output Buffer: off [2]; ODT: disabled [3]; Active Banks: All (during Self-Refresh action); Idle Banks: all (between Self-Rerefresh actions) |
| IDD6ET | Self-Refresh Current: extended temperature range<br>Tcase=0-95°C; Auto Self Refresh =Disable; Self Refresh Temperature Range=Extended[9]; CKE=Low; External Clock=Off (CK and CK: Low); CS, Command Inputs, Row, Column Address, Bank Address, Data I/O: Floating; Output Buffer: off [2]; ODT: disabled [3]; Active Banks: All (during Self-Refresh action); Idle Banks: all (between Self-Rerefresh actions) |
| IDD6TC | Auto Self-Refresh Current<br>Tcase=0-95°C; Auto Self Refresh =Enable[8]; Self Refresh Temperature Range=Normal[9]; CKE=Low; External Clock=Off (CK and CK: Low); CS, Command Inputs, Row, Column Address, Bank Address, Data I/O: Floating; Output Buffer: off [2]; ODT: disabled [3]; Active Banks: All (during Self-Refresh action); Idle Banks: all (between Self-Rerefresh actions) |
| IDD7 | Operating Bank Interleave Read Current<br>CKE=High; External Clock=On; tCK, tRC, tRAS, tRCD, tRRD, CL: see table as below; AL=tRCD.min-tCK; CS=High between valid commands; Command Input: see table; Row, Column Address: Stable during DESELECT; Bank Address: cycling[10]; Data I/O: Read Data: Output Data switches every clock cycle (i.e. data stable during one clock cycle); Output Buffer: Off [2];ODT: disabled [3]; Burst Length: BL8; Active / Idle Banks: All [10] / none. |

Note1: SWITCHING for Address and Command Input Signals as described in Definition of SWITCHING for Address and Command Input Signals Table.
Note2: Output Buffer off: set MR1 A[12] = 1
Note3: ODT disable: set MR1 A[9,6,2]=000 and MR2 A[10,9]=00
Note4: Definition of D and D: described in Definition of SWITCHING for Address and Command Input Signals Table; Ax/Rx/Wx: Activate/Read/Write to Bank x.
Note5: BL8 fixed by MRS: set MR0 A[1,0]=00
Note6: Precharge Power Down Mode: set MR0 A12=0/1 for Slow/Fast Exit
Note7: Because it is an exit after precharge power down, the valid commands are: ACT, REF, MRS, Enter Self-Refresh.
Note8: Auto Self-Refresh(ASR): set MR2 A6 = 0/1 to disable/enable feature
Note9: Self-Refresh Temperature Range (SRT): set MR2 A7 = 0/1 for normal/extended temperature range
Note10: Cycle banks as follows: 0,1,2,3,...,7,0,1,...

## For ID testing the following parameters are utilized.

## For testing the IDD parameters, the following timing parameters are used:

| Parameter | | Symbol | DDR3-800 | | DDR3-1066 | DDR3-1333 | DDR3-1600 | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| | | | -5-5-5 | -6-6-6 | -7-7-7 | -9-9-9 | -11-11-11 | |
| Clock Cycle Time | | tCKmin(IDD) | 2.5 | 2.5 | 1.875 | 1.5 | 1.25 | ns |
| CAS Latency | | CL(IDD) | 5 | 6 | 7 | 9 | 11 | nCK |
| Active to Read or Write delay | | tRCDmin(IDD) | 12.5 | 15 | 13.125 | 12 | 13.125 | ns |
| Active to Active / Auto-Refresh command period | | tRCmin(IDD) | 50 | 52.5 | 50.63 | 48 | 48.125 | ns |
| Active to Precharge Command | | tRASmin(IDD) | 37.5 | 37.5 | 37.5 | 36 | 35 | ns |
| Precharge Command Period | | tRPmin(IDD) | 12.5 | 15 | 13.13 | 12 | 13.75 | ns |
| Four activate window | 1kB | tFAW(IDD) | 40 | 40 | 37.5 | 30 | 30 | ns |
| | 2kB | | 50 | 50 | 50 | 45 | 40 | ns |
| Active to Active command period | 1kB | tRRD(IDD) | 10 | 10 | 7.5 | 6 | 6 | nCK |
| | 2kB | | 10 | 10 | 10 | 7.5 | 7.5 | nCK |
| Auto-Refresh to Active / Auto-Refresh command period | | tRFC(IDD) | 160 | 160 | 160 | 160 | 160 | ns |

## Definition of SWITCHING for Address and Command Input Signals

| SWITCHING for Address (row, column) and Command Signals (CS, RAS, CAS, WE) is defined as: | |
|---|---|
| Address<br>(row, column) | If not otherwise mentioned the inputs are stable at HIGH or LOW during 4 clocks and change then to the opposite value<br>(e.g. Ax Ax Ax Ax $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ Ax Ax Ax Ax…<br>Please see each IDDx definition for details |
| Bank Address | If not otherwise mentioned the bank addresses should be switched like the row/column address - please see each IDDx for details |
| Command<br>($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) | Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$} := {HIGH, LOW, LOW, LOW}<br>Define D = { $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ } := {HIGH, HIGH, HIGH, HIGH}<br>Define Command Background Pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$....<br>If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R), the Background Pattern Command is substituted by the respective $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ levels of the necessary command. See each IDDx definition for details. |

## Standard Speed Bins

### DDR3-1600MHz

| Speed Bin | | | DDR3-1600 | | Unit |
|---|---|---|---|---|---|
| CL-nRCD-nRP | | | 11-11-11 | | Unit |
| Parameter | | Symbol | Min | Max | |
| Internal read command to first data | | tAA | 13.750<br>(13.125)[5,11] | 20.000 | ns |
| ACT to internal read or write delay time | | tRCD | 13.750<br>(13.125)[5,11] | - | ns |
| PRE command period | | tRP | 13.750<br>(13.125)[5,11] | - | ns |
| ACT to ACT or REF command period | | tRC | 48.750<br>(48.125)[5,11] | - | ns |
| ACT to PRE command period | | tRAS | 35.000 | 9*tREFI | ns |
| CL=5 | CWL =5 | tCK(AVG) | 3.000 | 3.300 | ns |
| | CWL =6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =7 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =8 | tCK(AVG) | Reserved | Reserved | ns |
| CL=6 | CWL =5 | tCK(AVG) | 2.500 | 3.300 | ns |
| | CWL =6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =7 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =8 | tCK(AVG) | Reserved | Reserved | ns |
| CL=7 | CWL =5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =6 | tCK(AVG) | 1.875 | <2.5 | ns |
| | CWL =7 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =8 | tCK(AVG) | Reserved | Reserved | ns |
| CL=8 | CWL =5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =6 | tCK(AVG) | 1.875 | <2.5 | ns |
| | CWL =7 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =8 | tCK(AVG) | Reserved | Reserved | ns |
| CL=9 | CWL =5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =7 | tCK(AVG) | 1.500 | <1.875 | ns |
| | CWL =8 | tCK(AVG) | Reserved | Reserved | ns |
| CL=10 | CWL =5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =7 | tCK(AVG) | 1.500 | <1.875 | ns |
| | CWL =8 | tCK(AVG) | 1.250 | <1.5 | ns |
| CL=11 | CWL =5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =7 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL =8 | tCK(AVG) | 1.250* | <1.5* | ns |
| Supported CL Settings | | | 6,7,8,9,10,(11) | | nCK |
| Supported CWL Settings | | | 5,6,7,8 | | nCK |
| *: Optional | | | | | |

## DDR3-1333MHz

| Speed Bin | | | DDR3-1333 | | Unit |
|---|---|---|---|---|---|
| CL-nRCD-nRP | | | 9-9-9 (-CG) | | |
| Parameter | | Symbol | Min | Max | |
| Internal read command to first data | | tAA | 13.125 | 20.000 | ns |
| ACT to internal read or write delay time | | tRCD | 13.125 | - | ns |
| PRE command period | | tRP | 13.125 | - | ns |
| ACT to ACT or REF command period | | tRC | 49.125 | - | ns |
| ACT to PRE command period | | tRAS | 36.000 | 9*tREFI | ns |
| CL=5 | CWL=5 | tCK(AVG) | 3.000 | 3.300 | ns |
| | CWL=6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=7 | tCK(AVG) | Reserved | Reserved | ns |
| CL=6 | CWL=5 | tCK(AVG) | 2.500 | 3.300 | ns |
| | CWL=6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=7 | tCK(AVG) | Reserved | Reserved | ns |
| CL=7 | CWL=5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=6 | tCK(AVG) | 1.875* | <2.5* | ns |
| | CWL=7 | tCK(AVG) | Reserved | Reserved | ns |
| CL=8 | CWL=5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=6 | tCK(AVG) | 1.875 | <2.5 | ns |
| | CWL=7 | tCK(AVG) | Reserved | Reserved | ns |
| CL=9 | CWL=5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=7 | tCK(AVG) | 1.500 | <1.875 | ns |
| CL=10 | CWL=5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=7 | tCK(AVG) | 1.500* | <1.875* | ns |
| Supported CL Settings | | | 6,7,8,9,(10) | | nCK |
| Supported CWL Settings | | | 5,6,7 | | nCK |

## Electrical Characteristics & AC Timing

## Timing Parameter by Speed Bin (DDR3-800, 1066MHz)

| Parameter | Symbol | DDR3-800 | | DDR3-1066 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Clock Timing | | | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK (DLL_OFF) | 8 | - | 8 | - | ns | |
| Average Clock Period | tCK(avg) | Refer to "Standard Speed Bins) | | | | ps | |
| Average high pulse width | tCH(avg) | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) | |
| Absolute Clock Period | tCK(abs) | Min.: tCK(avg)min + tJIT(per)min<br>Max.: tCK(avg)max + tJIT(per)max | | | | ps | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.43 | - | 0.43 | - | tCK(avg) | |
| Absolute clock LOW pulse width | tCL(abs) | 0.43 | - | 0.43 | - | tCK(avg) | |
| Clock Period Jitter | JIT(per) | -100 | 100 | -90 | 90 | ps | |
| Clock Period Jitter during DLL locking period | JIT(per, lck) | -90 | 90 | -80 | 80 | ps | |
| Cycle to Cycle Period Jitter | tJIT(cc) | 200 | 200 | 180 | 180 | ps | |
| Cycle to Cycle Period Jitter during DLL locking period | JIT(cc, lck) | 180 | 180 | 160 | 160 | ps | |
| Duty Cycle Jitter | tJIT(duty) | - | - | - | - | ps | |
| Cumulative error across 2 cycles | tERR(2per) | -147 | 147 | -132 | 132 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | -175 | 175 | -157 | 157 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | -194 | 194 | -175 | 175 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | -209 | 209 | -188 | 188 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | -222 | 222 | -200 | 200 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | -232 | 232 | -209 | 209 | ps | |
| Cumulative error across 8 cycles | tERR(8per) | -241 | 241 | -217 | 217 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | -249 | 249 | -224 | 224 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | -257 | 257 | -231 | 231 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | -263 | 263 | -237 | 237 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | -269 | 269 | -242 | 242 | ps | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper) | tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min<br>tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max | | | | ps | |
| Data Timing | | | | | | | |
| DQS, DQS# to DQ skew, per group, per access | tDQSQ | - | 200 | - | 150 | ps | |
| DQ output hold time from DQS, DQS# | tQH | 0.38 | - | 0.38 | - | tCK(avg) | |
| DQ low-impedance time from CK, CK# | tLZ(DQ) | -800 | 400 | -600 | 300 | ps | |
| DQ high impedance time from CK, CK# | tHZ(DQ) | - | 400 | - | 300 | ps | |
| Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | tDS(base) AC175 | 75 | | 25 | | ps | |
| Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | tDS(base) AC150 | 125 | | 75 | | ps | |
| Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels | tDH(base) DC100 | 150 | | 100 | | ps | |
| DQ and DM Input pulse width for each input | tDIPW | 600 | | 490 | | ps | |
| Data Strobe Timing | | | | | | | |
| DQS,DQS# differential READ Preamble | tRPRE | 0.9 | Note 19 | 0.9 | Note 19 | tCK(avg) | |
| DQS, DQS# differential READ Postamble | tRPST | 0.3 | Note 11 | 0.3 | Note 11 | tCK(avg) | |
| DQS, DQS# differential output high time | tQSH | 0.38 | - | 0.38 | - | tCK(avg) | |
| DQS, DQS# differential output low time | tQSL | 0.38 | - | 0.38 | - | tCK(avg) | |
| DQS, DQS# differential WRITE Preamble | tWPRE | 0.9 | - | 0.9 | - | tCK(avg) | |
| DQS, DQS# differential WRITE Postamble | tWPST | 0.3 | - | 0.3 | - | tCK(avg) | |
| DQS, DQS# rising edge output access time from rising CK, CK# | tDQSCK | -400 | 400 | -300 | 300 | tCK(avg) | |
| DQS and DQS# low-impedance time (Referenced from RL - 1) | tLZ(DQS) | -800 | 400 | -600 | 300 | tCK(avg) | |
| DQS and DQS# high-impedance time (Referenced from RL + BL/2) | tHZ(DQS) | - | 400 | - | 300 | tCK(avg) | |
| DQS, DQS# differential input low pulse width | tDQSL | 0.45 | 0.55 | 0.45 | 0.55 | tCK(avg) | |
| DQS, DQS# differential input high pulse width | tDQSH | 0.45 | 0.55 | 0.45 | 0.55 | tCK(avg) | |
| DQS, DQS# rising edge to CK, CK# rising edge | tDQSS | -0.25 | 0.25 | -0.25 | 0.25 | tCK(avg) | |
| DQS, DQS# falling edge setup time to CK, CK# rising edge | tDSS | 0.2 | - | 0.2 | - | tCK(avg) | |
| DQS, DQS# falling edge hold time from CK, CK# rising edge | tDSH | 0.2 | - | 0.2 | - | tCK(avg) | |
| Command and Address Timing | | | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DLL locking time | tDLLK | 512 | - | 512 | - | nCK | |
| Internal READ Command to PRECHARGE Command delay | tRTP | tRTPmin.: max(4nCK, 7.5ns)<br>tRTPmax.: - | | | | | |
| Delay from start of internal write transaction to internal read command | tWTR | tWTRmin.: max(4nCK, 7.5ns)<br>tWTRmax.: | | | | | |
| WRITE recovery time | tWR | 15 | - | 15 | - | ns | |
| Mode Register Set command cycle time | tMRD | 4 | - | 4 | - | nCK | |
| Mode Register Set command update delay | tMOD | tMODmin.: max(12nCK, 15ns)<br>tMODmax.: | | | | | |
| ACT to internal read or write delay time | tRCD | | | | | | |
| PRE command period | tRP | | | | | | |
| ACT to ACT or REF command period | tRC | | | | | | |
| CAS# to CAS# command delay | tCCD | 4 | - | 4 | - | nCK | |
| Auto precharge write recovery + precharge time | tDAL(min) | WR + roundup(tRP / tCK(avg)) | | | | nCK | |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | 1 | - | nCK | |
| ACTIVE to PRECHARGE command period | tRAS | Standard Speed Bins | | | | | |
| ACTIVE to ACTIVE command period for 1KB page size | tRRD | max(4nCK, 10ns) | - | max(4nCK, 7.5ns) | - | | |
| ACTIVE to ACTIVE command period for 2KB page size | tRRD | tRRDmin.: max(4nCK, 10ns)<br>tRRDmax.: | | | | | |
| Four activate window for 1KB page size | tFAW | 40 | - | 37.5 | - | ns | |
| Four activate window for 2KB page size | tFAW | 50 | - | 50 | - | ns | |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 200 | - | 125 | - | ps | |
| Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels | tIH(base) | 275 | - | 200 | - | ps | |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) AC150 | 200+150 | - | 125+150 | - | ps | |
| Control and Address Input pulse width for each input | tIPW | 900 | - | 780 | - | ps | |
| Calibration Timing | | | - | | | | |
| Power-up and RESET calibration time | tZQinit | 512 | - | 512 | - | nCK | |
| Normal operation Full calibration time | tZQoper | 256 | - | 256 | - | nCK | |
| Normal operation Short calibration time | tZQCS | 64 | - | 64 | - | nCK | |
| Reset Timing | | | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | tXPRmin.: max(5nCK, tRFC(min) + 10ns)<br>tXPRmax.: - | | | | | |
| Self Refresh Timings | | | | | | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | tXSmin.: max(5nCK, tRFC(min) + 10ns)<br>tXSmax.: - | | | | | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tXSDLLmin.: tDLLK(min)<br>tXSDLLmax.: - | | | | nCK | |
| Minimum CKE low width for Self Refresh entry to exit timing | tCKESR | tCKESRmin.: tCKE(min) + 1 nCK<br>tCKESRmax.: - | | | | | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | tCKSREmin.: max(5 nCK, 10 ns)<br>tCKSREmax.: - | | | | | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | tCKSRXmin.: max(5 nCK, 10 ns)<br>tCKSRXmax.: - | | | | | |
| Power Down Timings | | | | | | | |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | tXPmin.: max(3nCK, 7.5ns)<br>tXPmax.: - | | | | | |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL | tXPDLL | tXPDLLmin.: max(10nCK, 24ns)<br>tXPDLLmax.: - | | | | | |
| CKE minimum pulse width | tCKE | tCKEmin.: max(3nCK 7.5ns)<br>tCKEmax.: - | | tCKEmin.: max(3nCK 5.625ns)<br>tCKEmax.: - | | | |
| Command pass disable delay | tCPDED | tCPDEDmin.: 1<br>tCPDEDmin.: - | | | | nCK | |
| Power Down Entry to Exit Timing | tPD | tPDmin.: tCKE(min)<br>tPDmax.: 9*tREFI | | | | | |
| Timing of ACT command to Power Down entry | tACTPDEN | tACTPDENmin.: 1<br>tACTPDENmax.: - | | | | nCK | |
| Timing of PRE or PREA command to Power Down entry | tPRPDEN | tPRPDENmin.: 1<br>tPRPDENmax.: - | | | | nCK | |
| Timing of RD/RDA command to Power Down entry | tRDPDEN | tRDPDENmin.: RL+4+1 | | | | nCK | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | tRDPDENmax.: - | | | | | |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | tWRPDENmin.: WL + 4 + (tWR / tCK(avg))<br>tWRPDENmax.: - | | | | nCK | |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | tWRAPDENmin.: WL+4+WR+1<br>tWRAPDENmax.: - | | | | nCK | |
| Timing of WR command to Power Down entry (BC4MRS) | tWRPDEN | tWRPDENmin.: WL + 2 + (tWR / tCK(avg))tWRPDENmax.: - | | | | nCK | |
| Timing of WRA command to Power Down entry (BC4MRS) | tWRAPDEN | tWRAPDENmin.: WL + 2 +WR + 1<br>tWRAPDENmax.: - | | | | nCK | |
| Timing of REF command to Power Down entry | tREFPDEN | tREFPDENmin.: 1<br>tREFPDENmax.: - | | | | nCK | |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMRSPDENmin.: tMOD(min)<br>tMRSPDENmax.: - | | | | | |
| ODT Timings | | | | | | | |
| ODT high time without write command or with write command and BC4 | ODTH4 | ODTH4min.: 4<br>ODTH4max.: - | | | | nCK | |
| ODT high time with Write command and BL8 | ODTH8 | ODTH8min.: 6<br>ODTH8max.: - | | | | nCK | |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONPD | 2 | 8.5 | 2 | 8.5 | ns | |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFPD | 2 | 8.5 | 2 | 8.5 | ns | |
| RTT turn-on | tAON | -400 | 400 | -300 | 300 | ps | |
| RTT_Nom and RTT_WR turn-off time from ODTLoff reference | tAOF | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | |
| Write Leveling Timings | | | | | | | |
| First DQS/DQS# rising edge after write leveling mode is programmed | tWLMRD | 40 | - | 40 | - | nCK | |
| DQS/DQS# delay after write leveling mode is programmed | tWLDQSEN | 25 | - | 25 | - | nCK | |
| Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing | tWLS | 325 | - | 245 | - | ps | |
| Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing | tWLH | 325 | - | 245 | - | ps | |
| Write leveling output delay | tWLO | 0 | 9 | 0 | 9 | ns | |
| Write leveling output error | tWLOE | 0 | 2 | 0 | 2 | ns | |

## Timing Parameter by Speed Bin (DDR3-1333, 1600MHz)

| Parameter | Symbol | DDR3-1333 | | DDR3-1600 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Clock Timing | | | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK (DLL_OFF) | 8 | - | 8 | - | ns | |
| Average Clock Period | tCK(avg) | Refer to "Standard Speed Bins) | | | | ps | |
| Average high pulse width | tCH(avg) | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) | |
| Absolute Clock Period | tCK(abs) | Min.: tCK(avg)min + tJIT(per)min<br>Max.: tCK(avg)max + tJIT(per)max | | | | ps | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.43 | - | 0.43 | - | tCK(avg) | |
| Absolute clock LOW pulse width | tCL(abs) | 0.43 | - | 0.43 | - | tCK(avg) | |
| Clock Period Jitter | JIT(per) | -80 | 80 | -70 | 70 | ps | |
| Clock Period Jitter during DLL locking period | JIT(per, lck) | -70 | 70 | -60 | 60 | ps | |
| Cycle to Cycle Period Jitter | tJIT(cc) | 160 | 160 | 140 | 140 | ps | |
| Cycle to Cycle Period Jitter during DLL locking period | JIT(cc, lck) | 140 | 140 | 120 | 120 | ps | |
| Duty Cycle Jitter | tJIT(duty) | - | - | - | - | ps | |
| Cumulative error across 2 cycles | tERR(2per) | -118 | 118 | -103 | 103 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | -140 | 140 | -122 | 122 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | -155 | 155 | -136 | 136 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | -168 | 168 | -147 | 147 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | -177 | 177 | -155 | 155 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | -186 | 186 | -163 | 163 | ps | |
| Cumulative error across 8 cycles | tERR(8per) | -193 | 193 | -169 | 169 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | -200 | 200 | -175 | 175 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | -205 | 205 | -180 | 180 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | -210 | 210 | -184 | 184 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | -215 | 215 | -188 | 188 | ps | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper) | tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min<br>tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max | | | | ps | |
| Data Timing | | | | | | | |
| DQS, DQS# to DQ skew, per group, per access | tDQSQ | - | 125 | - | 100 | ps | |
| DQ output hold time from DQS, DQS# | tQH | 0.38 | - | 0.38 | - | tCK(avg) | |
| DQ low-impedance time from CK, CK# | tLZ(DQ) | -500 | 250 | -450 | 225 | ps | |
| DQ high impedance time from CK, CK# | tHZ(DQ) | - | 250 | - | 225 | ps | |
| Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | tDS(base) AC175 | - | | - | | ps | |
| Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | tDS(base) AC150 | 30 | | 10 | | ps | |
| Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels | tDH(base) DC100 | 65 | | 45 | | ps | |
| DQ and DM Input pulse width for each input | tDIPW | 400 | - | 360 | | ps | |
| Data Strobe Timing | | | | | | | |
| DQS,DQS# differential READ Preamble | tRPRE | 0.9 | Note 19 | 0.9 | Note 19 | tCK(avg) | |
| DQS, DQS# differential READ Postamble | tRPST | 0.3 | Note 11 | 0.3 | Note 11 | tCK(avg) | |
| DQS, DQS# differential output high time | tQSH | 0.4 | - | 0.4 | - | tCK(avg) | |
| DQS, DQS# differential output low time | tQSL | 0.4 | - | 0.4 | - | tCK(avg) | |
| DQS, DQS# differential WRITE Preamble | tWPRE | 0.9 | - | 0.9 | - | tCK(avg) | |
| DQS, DQS# differential WRITE Postamble | tWPST | 0.3 | - | 0.3 | - | tCK(avg) | |
| DQS, DQS# rising edge output access time from rising CK, CK# | tDQSCK | -255 | 255 | -225 | 225 | tCK(avg) | |
| DQS and DQS# low-impedance time (Referenced from RL - 1) | tLZ(DQS) | -500 | 250 | -450 | 225 | tCK(avg) | |
| DQS and DQS# high-impedance time (Referenced from RL + BL/2) | tHZ(DQS) | - | 250 | - | 225 | tCK(avg) | |
| DQS, DQS# differential input low pulse width | tDQSL | 0.45 | 0.55 | 0.45 | 0.55 | tCK(avg) | |
| DQS, DQS# differential input high pulse width | tDQSH | 0.45 | 0.55 | 0.45 | 0.55 | tCK(avg) | |
| DQS, DQS# rising edge to CK, CK# rising edge | tDQSS | -0.25 | 0.25 | -0.27 | 0.27 | tCK(avg) | |
| DQS, DQS# falling edge setup time to CK, CK# rising edge | tDSS | 0.2 | - | 0.18 | - | tCK(avg) | |
| DQS, DQS# falling edge hold time from CK, CK# rising edge | tDSH | 0.2 | - | 0.18 | - | tCK(avg) | |
| Command and Address Timing | | | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DLL locking time | tDLLK | 512 | - | 512 | - | nCK | |
| Internal READ Command to PRECHARGE Command delay | tRTP | tRTPmin.: max(4nCK, 7.5ns)<br>tRTPmax.: - | | | | | |
| Delay from start of internal write transaction to internal read command | tWTR | tWTRmin.: max(4nCK, 7.5ns)<br>tWTRmax.: | | | | | |
| WRITE recovery time | tWR | 15 | - | 15 | - | ns | |
| Mode Register Set command cycle time | tMRD | 4 | - | 4 | - | nCK | |
| Mode Register Set command update delay | tMOD | tMODmin.: max(12nCK, 15ns)<br>tMODmax.: | | | | | |
| ACT to internal read or write delay time | tRCD | | | | | | |
| PRE command period | tRP | | | | | | |
| ACT to ACT or REF command period | tRC | | | | | | |
| CAS# to CAS# command delay | tCCD | 4 | - | 4 | - | nCK | |
| Auto precharge write recovery + precharge time | tDAL(min) | WR + roundup(tRP / tCK(avg)) | | | | nCK | |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | 1 | - | nCK | |
| ACTIVE to PRECHARGE command period | tRAS | Standard Speed Bins | | | | | |
| ACTIVE to ACTIVE command period for 1KB page size | tRRD | tRRDmin.: max(4nCK, 6ns)<br>tRRDmax.: | | | | | |
| ACTIVE to ACTIVE command period for 2KB page size | tRRD | tRRDmin.: max(4nCK, 7.5ns)<br>tRRDmax.: | | | | | |
| Four activate window for 1KB page size | tFAW | 30 | 0 | 30 | - | ns | |
| Four activate window for 2KB page size | tFAW | 45 | 0 | 40 | - | ns | |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 65 | - | 45 | - | ps | |
| Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels | tIH(base) | 140 | - | 120 | - | ps | |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) AC150 | 65+125 | - | 170 | - | ps | |
| Control and Address Input pulse width for each input | tIPW | 620 | - | 560 | - | ps | |
| Calibration Timing | | | | | | | |
| Power-up and RESET calibration time | tZQinit | 512 | - | 512 | - | nCK | |
| Normal operation Full calibration time | tZQoper | 256 | - | 256 | - | nCK | |
| Normal operation Short calibration time | tZQCS | 64 | - | 64 | - | nCK | |
| Reset Timing | | | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | tXPRmin.: max(5nCK, tRFC(min) + 10ns)<br>tXPRmax.: - | | | | | |
| Self Refresh Timings | | | | | | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | tXSmin.: max(5nCK, tRFC(min) + 10ns)<br>tXSmax.: - | | | | | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tXSDLLmin.: tDLLK(min)<br>tXSDLLmax.: - | | | | nCK | |
| Minimum CKE low width for Self Refresh entry to exit timing | tCKESR | tCKESRmin.: tCKE(min) + 1 nCK<br>tCKESRmax.: - | | | | | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | tCKSREmin.: max(5 nCK, 10 ns)<br>tCKSREmax.: - | | | | | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | tCKSRXmin.: max(5 nCK, 10 ns)<br>tCKSRXmax.: - | | | | | |
| Power Down Timings | | | | | | | |
| Exit Power Down with DLL on to any valid command;<br>Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | tXPmin.: max(3nCK, 6ns)<br>tXPmax.: - | | tXPmin.: max(3nCK, 6ns)<br>tXPmax.: - | | | |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL | tXPDLL | tXPDLLmin.: max(10nCK, 24ns)<br>tXPDLLmax.: - | | | | | |
| CKE minimum pulse width | tCKE | tCKEmin.: max(3nCK ,5.625ns)<br>tCKEmax.: - | | tCKEmin.: max(3nCK ,5ns)<br>tCKEmax.: - | | | |
| Command pass disable delay | tCPDED | tCPDEDmin.: 1<br>tCPDEDmin.: - | | | | nCK | |
| Power Down Entry to Exit Timing | tPD | tPDmin.: tCKE(min)<br>tPDmax.: 9*tREFI | | | | | |
| Timing of ACT command to Power Down entry | tACTPDEN | tACTPDENmin.: 1<br>tACTPDENmax.: - | | | | nCK | |
| Timing of PRE or PREA command to Power Down entry | tPRPDEN | tPRPDENmin.: 1<br>tPRPDENmax.: - | | | | nCK | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Timing of RD/RDA command to Power Down entry | tRDPDEN | tRDPDENmin.: RL+4+1<br>tRDPDENmax.: - | | | | nCK | |
| Timing of WR command to Power Down entry<br>(BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | tWRPDENmin.: WL + 4 + (tWR / tCK(avg))<br>tWRPDENmax.: - | | | | nCK | |
| Timing of WRA command to Power Down entry<br>(BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | tWRAPDENmin.: WL+4+WR+1<br>tWRAPDENmax.: - | | | | nCK | |
| Timing of WR command to Power Down entry (BC4MRS) | tWRPDEN | tWRPDENmin.: WL + 2 + (tWR / tCK(avg))tWRPDENmax.: - | | | | nCK | |
| Timing of WRA command to Power Down entry<br>(BC4MRS) | tWRAPDEN | tWRAPDENmin.: WL + 2 +WR + 1<br>tWRAPDENmax.: - | | | | nCK | |
| Timing of REF command to Power Down entry | tREFPDEN | tREFPDENmin.: 1<br>tREFPDENmax.: - | | | | nCK | |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMRSPDENmin.: tMOD(min)<br>tMRSPDENmax.: - | | | | | |
| ODT Timings | | | | | | | |
| ODT high time without write command or<br>with write command and BC4 | ODTH4 | ODTH4min.: 4<br>ODTH4max.: - | | | | nCK | |
| ODT high time with Write command and BL8 | ODTH8 | ODTH8min.: 6<br>ODTH8max.: - | | | | nCK | |
| Asynchronous RTT turn-on delay<br>(Power-Down with DLL frozen) | tAONPD | 2 | 8.5 | 2 | 8.5 | ns | |
| Asynchronous RTT turn-off delay<br>(Power-Down with DLL frozen) | tAOFPD | 2 | 8.5 | 2 | 8.5 | ns | |
| RTT turn-on | tAON | -250 | 250 | -225 | 225 | ps | |
| RTT_Nom and RTT_WR turn-off time<br>from ODTLoff reference | tAOF | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | |
| Write Leveling Timings | | | | | | | |
| First DQS/DQS# rising edge after<br>write leveling mode is programmed | tWLMRD | 40 | - | 40 | - | nCK | |
| DQS/DQS# delay after write leveling mode is programmed | tWLDQSEN | 25 | - | 25 | - | nCK | |
| Write leveling setup time from rising CK, CK#<br>crossing to rising DQS, DQS# crossing | tWLS | 195 | - | 165 | - | ps | |
| Write leveling hold time from rising DQS, DQS#<br>crossing to rising CK, CK# crossing | tWLH | 195 | - | 165 | - | ps | |
| Write leveling output delay | tWLO | 0 | 9 | 0 | 7.5 | ns | |
| Write leveling output error | tWLOE | 0 | 2 | 0 | 2 | ns | |

## Jitter Notes

Specific Note a

Unit “tCK(avg)” represents the actual tCK(avg) of the input clock under operation. Unit “nCK” represents one clock cycle of the input clock, counting the actual clock edges. ex) tMRD=4 [nCK] means; if one Mode Register Set command is registered at Tm, anther Mode Register Set command may be registered at Tm+4, even if (Tm+4-Tm) is 4 x tCK(avg) + tERR(4per), min.

Specific Note b

These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc) transition edge to its respective clock signal (CK/CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note c

These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)) crossing to its respective clock signal (CK, CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note d

These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)) crossing.

Specific Note e

For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{tPARAM[ns] / tCK(avg)[ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP = RU{tRP/tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP/tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6-Tm) is less than 15ns due to input clock jitter.

Specific Note f

When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper), act of the input clock, where 2 <= m <=12. (output derating are relative to the SDRAM input clock.)

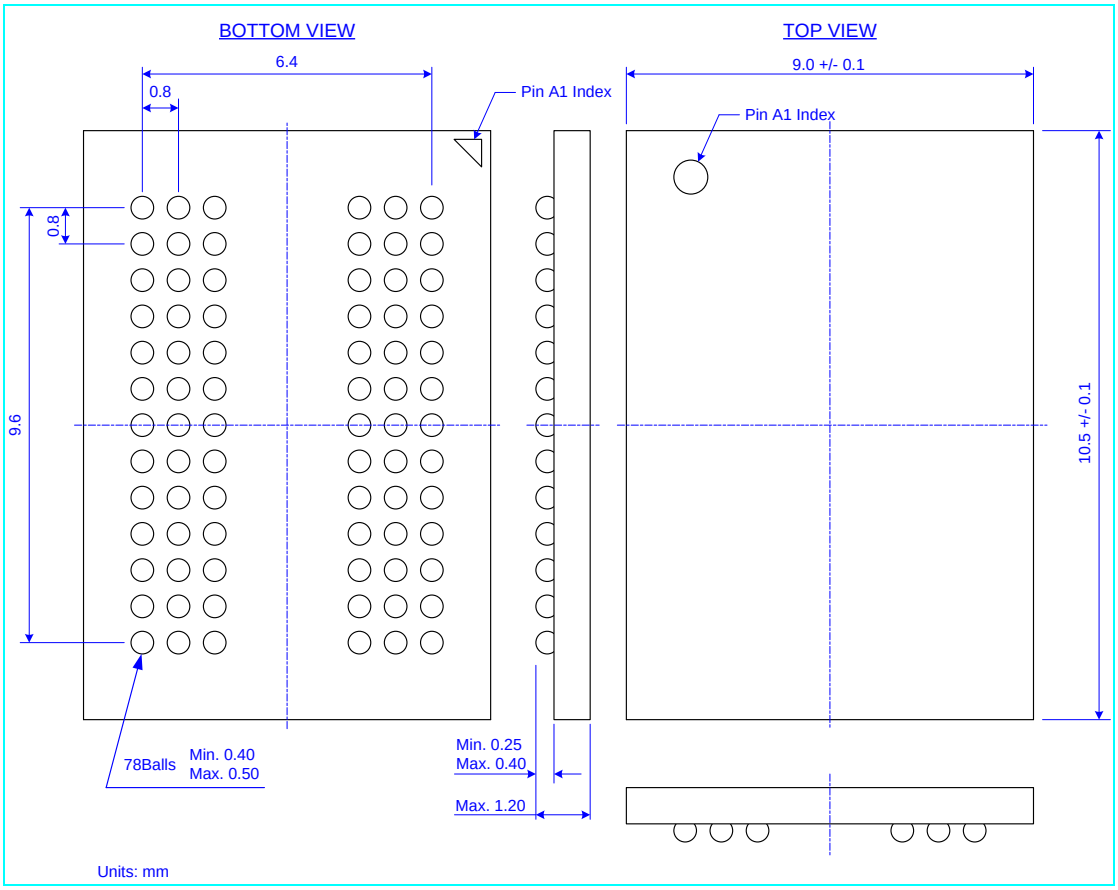
For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = -172ps and tERR(mper),act,max = 193ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = -400ps - 193ps = -593ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400ps + 172ps = 572ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = -800ps - 193ps = -993ps and tLZ(DQ),max(derated) = 400ps + 172ps = 572ps. (Caution on the min/max usage!)

Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12.

Specific Note g

When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act=2500ps, tJIT(per),act,min = -72ps and tJIT(per),act,max = 93ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500ps - 72ps = 2178ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500ps - 72ps = 878ps. (Caution on the min/max usage!)

## **Package Dimensions** (x8; 78 balls; 0.8mmx0.8mm Pitch; BGA)



## Package Dimensions (x16; 96 balls; 0.8mmx0.8mm Pitch; BGA)